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Zdzisław Nawrocki, Daniel Dusza

ANALOGUE AND DIGITAL MEASUREMENT SYSTEMS

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Contents

INTRODUCTION 7

PART I. Analog measurement systems 10

1. STRUCTURE OF ANALOG MEASUREMENT SYSTEMS 11

1.1. INTRODUCTION 11

1.2. SIGNAL PROCESSING IN ANALOG MEASUREMENT SYSTEMS 12

1.3. MEASUREMENT SYSTEM SIGNALS 13

1.4. SENSORS AND TRANSDUCERS SUPPLY WITH 4..20 mA OUTPUT CURRENT SIGNAL 14

2. SENSORS 16

3. CONVERTERS 19

3.1. INTRODUCTION 19

3.2. BASIC CIRCUITS WITH OPERATIONAL AMPLIFIERS 19

3.2.1. An inverting amplifier 19

3.2.2. A non-inverting amplifier 22

3.2.3. A voltage follower 23

3.2.4. A differential amplifier 24

3.3. PROPERTIES OF AMPLIFYING CIRCUITS WITH OPERATIONAL AMPLIFIERS 25

3.3.1. The input offset voltage and the offset current of operational amplifiers 26

3.3.2. Determine the effect of the input offset voltage and the bias currents for the amplifier output voltage 27

3.3.3 A circuit with operational amplifiers nulling 33

3.4 INSTRUMENTATION AMPLIFIERS 49

3.5. ISOLATION AMPLIFIERS 53

3.6. SIGNAL SWITCHES 59

4. MATHEMATICAL OPERATIONS REALIZING BY FUNCTIONAL CIRCUITS 61

4.1. INTRODUCTION 61

4.2. LOGARITHMIC AND EXPONENTIAL FUNCTIONS CIRCUITS 61

4.2.1. Principle of operation 61

4.2.2. Errors caused by elements of circuits 67

4.2.3. Logarithmic circuit realization 67

4.2.4. Exponential circuit realization 69

4.3. MULTIPLIER-DIVIDER CIRCUITS 70

4.4. MULTIFUNCTIONAL ANALOG TRANSDUCER 73

4.5. MULTIPLIERS WITH CONTROLLED CURRENTS DIVISION 77

4.5.1. Multipliers with controlled currents division - principle of operation .. 77

4.5.2. Use of multipliers with controlled currents division 82

4.6. TIME DIVISION MULTIPLIERS 88

4.7. ERRORS OF SIGNALS MULTIPLICATION AND DIVISION 92

4.7.1. Multiplier static errors 93

4.7.2. Divider static errors 94

4.8. DIVIDERS REALIZATION 95

4.9. SQUARER REALIZATION 96

4.10. SQUARE ROOTERS REALIZATION 98

4.11. MAXIMUM, MEAN, AND RMS VOLTAGE VALUE CONVERTERS 100

4.11.1. Maximum value converters 100

4.11.2. Mean value converter 103

4.11.3. RMS value converters 104

PART II. Digital measurement systems 111

5. DIGITAL MEASUREMENT SYSTEM - GENERAL INFORMATION 112

5.1. CLASSIFICATION, STRUCTURE AND ORGANIZATION OF DIGITAL MEASUREMENT SYSTEMS 112

5.2. FUNCTIONAL BLOCKS OF DIGITAL MEASURING SYSTEMS 118

5.2.1. A controller 118

5.2.2. User communication block 118

5.2.3. A measurement data acquisition block 118

5.2.4. A data processing block 125

5.2.5. A signal generation block 125

6. A/D AND D/A CONVERTERS 126

6.1. INTRODUCTION 126

6.2. A/D CONVERTERS 130

6.2.1. Flash converter 132

6.2.2. Serial with uniform rate compensation converters 134

6.2.3. A dual slope integrating A/D converter 136

6.2.4. Sigma – delta converter 138

6.3. D/A CONVERTERS 143

6.3.1. Binary-weighted D/A converter 144

6.2.1. R-2R D/A converter 144

6.4. COMPARISON OF ERRORS OF A/D AND D/A CONVERTERS 145

7. MEASUREMENT DISTURBANCES ATTENUATION 148

7.1. INTRODUCTION 148
7.2. TECHNIQUES OF DISTURBANCES ATTENUATION 150
7.2.1. Rejecting of the DC common-mode voltage 151
7.2.2. AC common-mode voltage rejecting 152
7.2.3. Break ground loops 153
7.2.4. 4-20mA current loops 154
7.2.5. 24 V digital logic 155
8. SENSORS AND TRANSDUCERS 157
8.1 INDUCTIVE CURRENT TRANSDUCERS AND SENSORS 157
8.2. SMART SENSORS 165
9. WIRELESS STRAY MEASUREMENT SYSTEMS 172
10. VIRTUAL INSTRUMENTS 180
11. CHOSEN MEASUREMENT SYSTEMS 192
REFERENCES 204

INTRODUCTION

Initially measurement systems help observer out in a difficult and time-consuming measurements and studies of the measurement results. With time, due to its properties:

- the high speed of operating,
- the large number of input and output data (the large information stream),
- right accuracy,

have become an essential part of the systems used in measurements, productive and technological processes.

For example production of the ferromagnetic materials called amorphous tapes requires precise and high-speed measurement system, which assures alloy cooling on the spinning barrel with the speed of 1000K during 1ms time and forming this product into tape. Data processing with that high speed and right accuracy assure only complex measurement systems.

The simplest and the most general definition describes the measurement system as a set of units creating the whole organizational system and serving one aim.

According to this definition the measurement system can be treated as a set of measurement equipment (measurement and additional devices) serving to receiving, processing, sending and remembering measuring information.

Generally the measurement system can be presented as a device with *n* inputs and *m* outputs (Fig. 1).

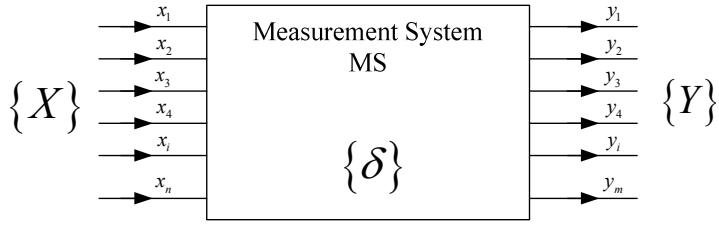


Fig. 1. Idea of measurement system
$\{X\}$ – information collects operator, $\{Y\}$ – input signals operator, $\{\delta\}$ – operator of the measurement system errors, x_i – input quantities, y_i – output quantities

Measurement system contains whole collection of means of acceptable errors δ realizing a relation

$$\{Y\} = F\left[\{X\},\{\delta\}\right], \tag{1}$$

where *F* is a function describing relations between the system input and output quantities, including operators of information collection, conversion, measurement and data processing and data preserve in relation to the accepted mathematical model (computing) and object "a priori" data.

The measurement system realizes algorithm of the measuring process showed in Fig. 2. The measurement process algorithm represents the basic actions sequence executed during measurements.

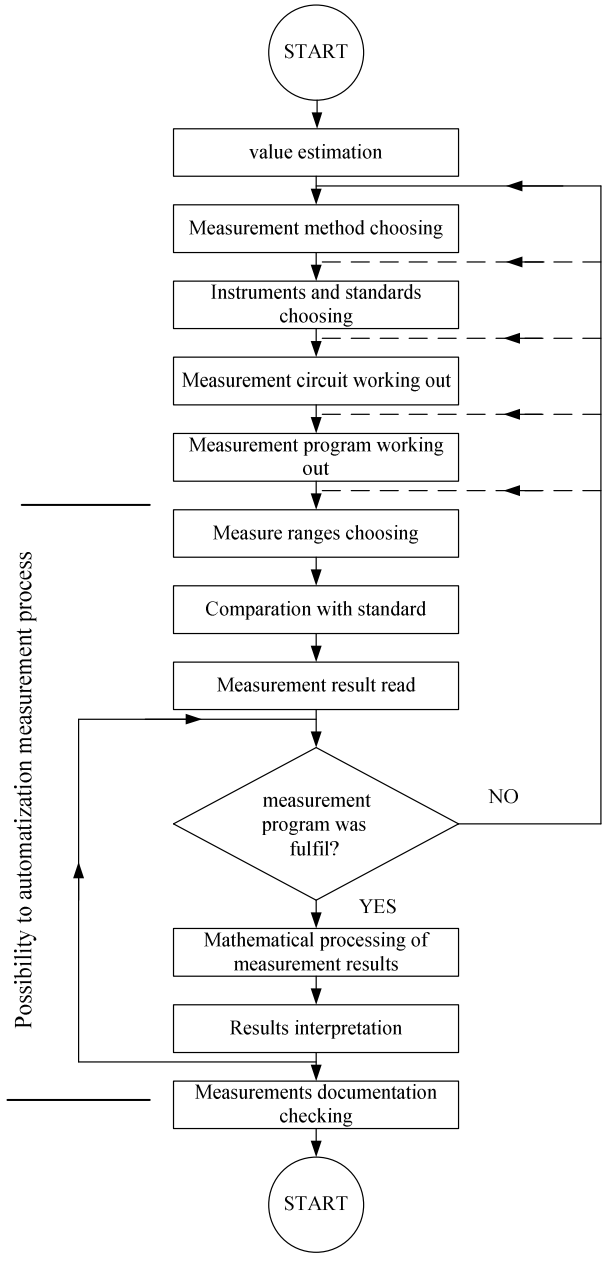


Fig. 2. Measurement process algorithm

The most time consuming part of the operations, described by the algorithm, on the choice of measurement ranges including the mathematical processing of measurement results can be automated.

The algorithm is realized by system including

- input devices units,
- central part, where the processing of measurement signals is occurred,
- output units.

Therefore is here two components of measurement system: hardware unit and software unit, co-operating in measuring task realization according to the user operation algorithm worked out.

In analog systems, automation of measurement process is implemented using combinational and sequential logic circuits, calculations are performed using the functional circuits, and storing results of the calculation is done using the static memory. In digital systems mentioned above operations are done with use of microcontrollers, microprocessors or controllers.

Measurement systems division

For the sake of processing signal form in the system, measurement systems can be divided into:

- analog,
- digital,
- analog-digital.

Measurement systems functional division

For the sake of fulfill metrological tasks, the measurements systems can be divided into three groups:

- laboratory-measurement systems,
- object control or technological processes systems, called monitoring systems,
- object testing systems, called diagnostics systems.

PART I

Analog measurement systems

1. STRUCTURE OF ANALOG MEASUREMENT SYSTEMS

1.1. INTRODUCTION

In the middle of the fiftieth of the last century works connected with study of conception and realization of analog measurement systems were undertaken. Disadvantage of these systems was use of the electro-mechanical parts (including moveable elements). Then, the measuring systems without moving parts based on different types of electronic converters and functional circuits was worked out. This systems bases on the various kinds of electronic transducers and functional circuits. In Poland principles of analog measurement system functioning was worked out in 1965. This system was called Universal Measurement System (UMS).

This system includes the set of measurement devices designed for continuous measurements, registration and signaling physic-chemical quantities, connected with production-technical processes, and also automatic of this processes needs. Structural circuit of that system is presented in Fig. 1.1.

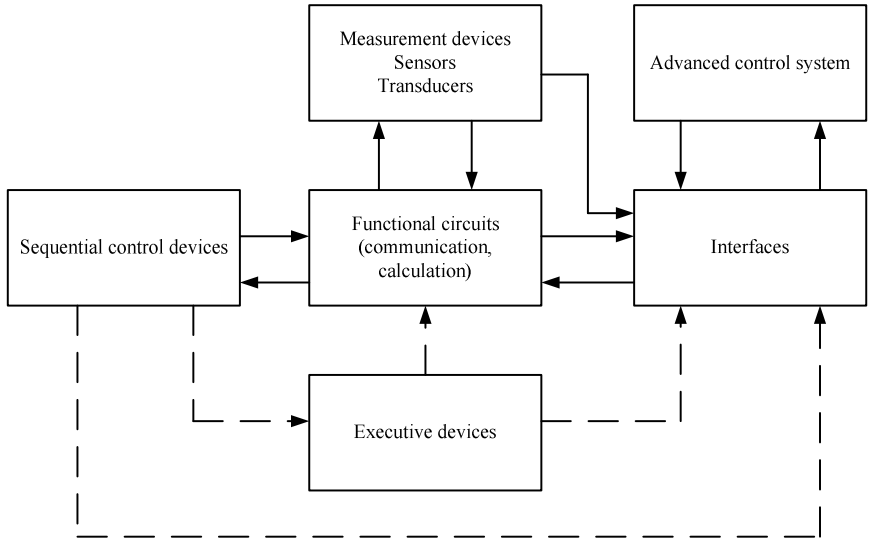


Fig. 1.1. A structural circuit of an analog measurement system

Nonelectric measuring quantities are exchanged with sensors to the electrical quantities and carried to measuring device. Next, an electrical quantities are normalized in the transducers, which also fulfill function of transmitters and then are sent to the central part of the system.

The central part of the system contains functional circuits which realizing mathematical operations like addition, subtraction, multiplication, division, extraction, raising, logarithmic, integration, differentiating, etc. These operations

are used on signals received from measurement devices. It can also contain comparators, logical structures defining input signals conditions and their relations. From central part are also controlled measuring transducers, in the aim of ranges changing, input signal levels and measure quantities choosing.

The output signals from the central part of the system control of automats and specialized devices Output signals from the central part of system control automats and specialized equipment. The control process can be realized by sequential control circuits. This signals with continuous or digital character can control executive devices. Information about executive device functions can be delivered to central part of the measurement system.

Signals from measuring devices, central part and executive equipment are transmitted to coupling device which has the connection with the central part and measurement device. These signals can also be used for a computerized control system to optional assist the analog measurement system.

1.2. SIGNAL PROCESSING IN ANALOG MEASUREMENT SYSTEMS

Most of the measured quantities generated by measurement objects have analog form and tentatively, even in digital measurement systems, are processing in an analog measurement line.

According to information from chapter 1.1 the measuring signal is taken by measurement device and is transmitted to the central part where is next processing.

Fig. 1.2 presents the measurement line consist of:

- sensors,
- transducers (normalizing),
- linear circuit - if the signal from the sensor is described by the non-linear function,
- transmitters (forcing current signal),
- multiplexer,
- transmission line,
- demultiplexer,
- functional circuits (analog computational unit) and remembering
- reading field,
- recorders *Xt* and *XY*.

Nonelectric measuring quantities $X_1, X_2,\ldots,X_n$ from tested object are transmitted to sensors to change this quantities into electric signals. Then this signals are normalized to standard value ranges in normalizing transducers. When the sensor has nonlinear characteristic then must be used additional linear circuit. On the next step the signals are transferred to transmitters, which output signal is defined by current output signal in range from 4mA to 20mA. This currents, through the multiplexer, transmission line and demultiplexer are received by part of the central system (Fig. 1.1) consist of functional circuits and remembering circuits. Processed output information of sensors can be illustrated on the reading field or can be recorded by recorders *Xt*, *XY* or transmitted to other components.

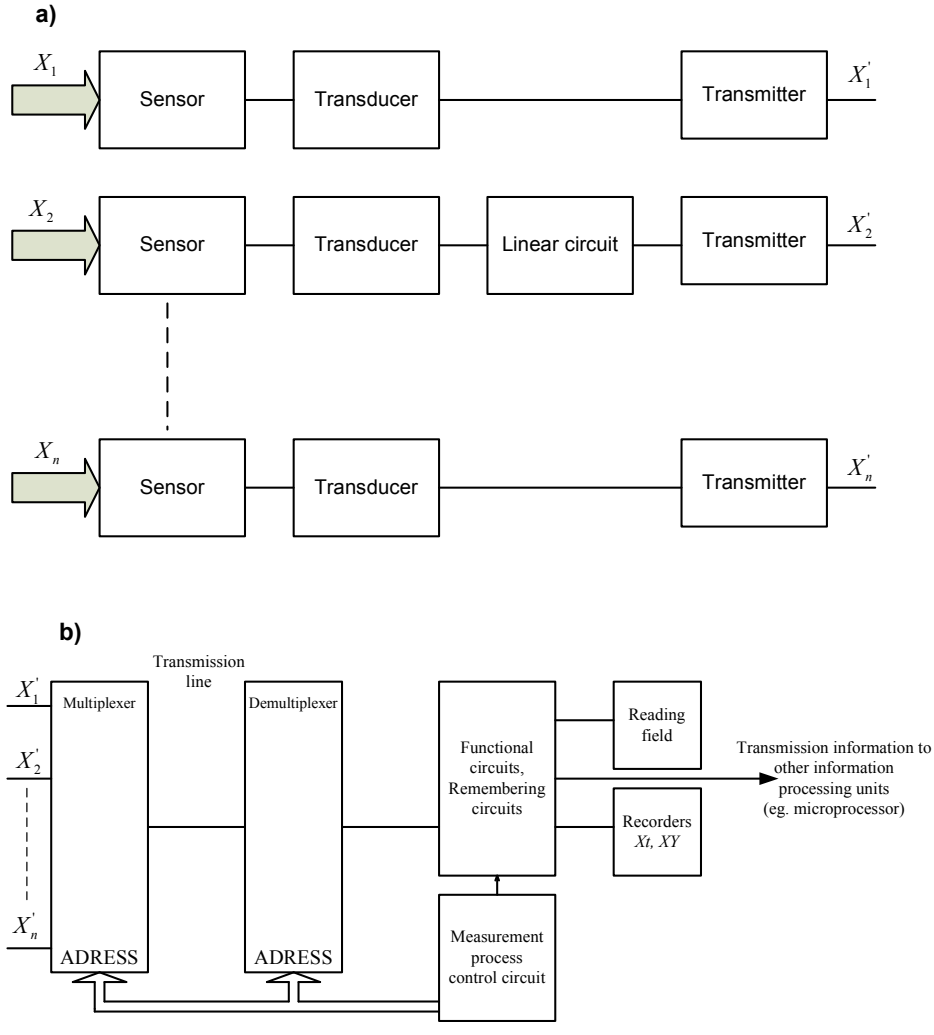


Fig. 1.2. An analog measurement system measurement line
a) input circuits, b) processing unit

1.3. MEASUREMENT SYSTEM SIGNALS

As the transfer signal sensors, transducers (transmitters) to the system central part and from system central part to executive elements the most often current signal (4..20)mA is assuming. This is the signal called as the "live zero". 4mA current value responds the "0" level of output sensor signal. Decrease current value to 0mA gives information about supply loss or sensor/transducer damage.

Because sensors with other transfer signals exists, so other current signals in system are admitted. Ranges of the values was presented in Table 1.1. In Table 1.1 was also shown voltage signals ranges applied in the system central part.

Tab.1.1. Standard signals and adequate to them transducers burden signals

No.	Standard signals	Burden
1	0...5 mA	≤2000 Ω
2	0…10 mA	≤1000 Ω
3	0…20 mA	≤500 Ω
4	4…20 mA	≤500 Ω
5	2…50 mA	≤100 Ω
6	-15 V…0…+15 V	≥1000 Ω

Information transmitting with current signals has a series of advantages. Current signal is insensitive on the changes of transfer line resistance, reduces influence of serial voltage disturbing sources, spark safety assures, and also allows on relatively easy power of transfer signal limitation. As it was presented in Table 1.1 the internal signal of system central part is voltage signal in range of -15 V..0..+15 V. This signal is a natural result of operational amplifiers use supplied by ±15 V voltage and has a lot of advantages. Among other things allows to use one supply with common zero rail in all components of system central part.

1.4. SENSORS AND TRANSDUCERS SUPPLY WITH 4..20 mA OUTPUT CURRENT SIGNAL

Sensor and transducers power supply with current signals at the beginning was, as it is shown in Fig. 1.3a, realized by 4 wired connections. Two wires was designed to supply, and other two to measurement signal transmission. Then the number of wires was reduced to three, upon that one of the wires, ground potential wire, is designed to supply the circuit and measurement signal transmission, as it is shown in Fig. 1.3b. Technological and circuitry progresses caused that sensors and transducers power consumption had reduced significantly. It was allowed to make the most of unused part of the current, the most often by values in range 3.8 mA to3.9 mA. 4..20 mA measuring signal is transmitted with uses the same wires as it was shown in Fig. 1.3c.

It should be signalizing, that very intensive research go on at present to supply the sensors and transmitters from stray energy sources. Power supply equipped with the correct converter processing the stray light, mechanical, acoustic energy occurs in the sensor/transducer and transmitter location and processing it into electrical energy.

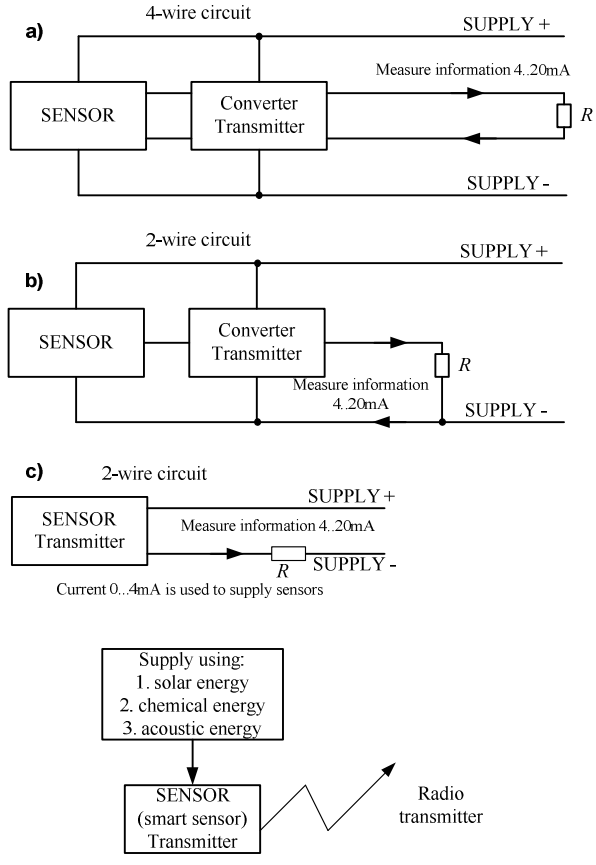


Fig. 1.3. Sensors and transducers supply with 4..20 mA output current signal
a) 4-wire circuit, b) 3-wire circuit, c) 2-wire circuit

This measurement units power consumption is very low, in the order of microwatts, and the measurement signals are radio transmitted as it is shown in Fig. 1.4.

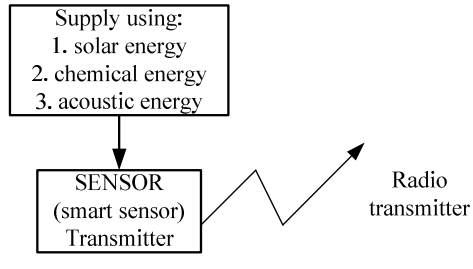


Fig. 1.4. Radio transmission of a sensor output signal

Designers have put a lot of effort into study and design electromagnetic field supply systems. For example with 800 MHz electromagnetic field could be supplied sensors, transducers and transmitters with 20 mW power consumption in the ray of 10 m.

2. SENSORS

Sensor is a measuring device designed for changes of nonelectrical physical quantity into electrical signal. Output signal from sensor or group of sensors is tentatively amplified (normalized) in normalizing transducers. Normalizing transducers are an operational amplifiers working, depends on sensor or sensors location, in non-inverting, inverting, differential, measuring-differential (instrumentation) configuration. In the case when the sensor must be galvanic separated from the measurement circuit then are used amplifiers with isolation barrier.

The list of sensors the most often applied in various physical quantities measurements is presented in Table 2.1 [22]. Detailed description of working principle and sensor properties goes beyond this book confines. It can be found in the literature [22].

Nowadays in the literature can there be found a few definitions of sensor. In this book there have been was presented two of them. First definition was presented by W. Kester in [7].

The main objective of sensors is to convert a signal or stimulus (representing a physical property) into an electrical output.

Other definition is given by the author of [28], which presents sensors as converters: converting one type of energy into another.

The second definition, presented in [32], who says that sensor is an element which allows receiving of information from a physical object. Parameters of this object must be identified in the measurement process.

The sample scheme of sensor processing function is shown in Fig. 2.1.

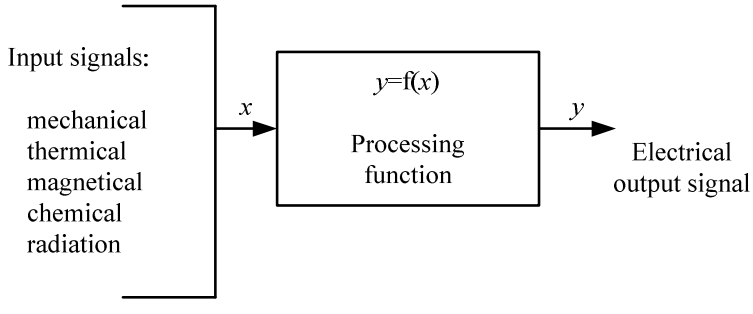


Fig. 2.1. Sensors processing function

Table 2.1. Physical laws use in sensors and transducers for various input and output quantities

Wy / We	Mechanical	Thermal	Magnetic	Electrical	Optical
Mechanical	Lever principle, pendulum, resilience effect	Thermal lengthen, (differential – bimetals), state transformations when V=const.	Amper law, magnetostriction	Coulomb law, electrostriction, piezoelectric effect	Radiation intensity
Thermal	Friction effect, adiabatic state transformations	Heat exchange	Eddy current effect	Joule heat, Dielectrically power dissipation, Peltier effect	Pyroelectrical effect
Magnetic	Magneto-resilience effect	Curie-Weiss effect	Magnetic remnant, hysteresis, dia-, para-, ferromagnetism	Biot-Sawart law	Curie-Weiss effect depending on absorption
Electrical	Piezoelectric effect	Temperature resistance dependence, thermoelectricity, pyroelectricity	Hall effect, magneto-resistance, Induction	Current flow in gases and liquids	External and internal photoelectric effect
Optical	Interference, modulation	Thermo-luminescence	Faraday effect, Zeeman effect	Keer effect, laser	Luminous flux modulation

On the base of kind of nonelectrical input quantities, sensors can be divided into two main groups:

- physical quantity sensors – they allow basic quantity measurements and their derivatives,
- chemical quantity sensors – they allow chemical composition analysis, define chemical reaction parameters, tests and estimations of the structure.

Other division of sensors can presented on the base of input signal to output signal processing and on the base of kind of the output signal:

- electronic sensors – principle of operation relies on electric charge reaction in the electrical or magnetic field,
- optical fibre sensors – input quantity is processed into light signal, which can be sent on large distances. Then the signal is processed back into the electrical signal.

Nowadays many of new designed sensors are produced as smart sensors. This kind of sensors is characterized by integrated processing circuits and signal standardization circuits. Usually they have integrated standard interface which allows to connect the sensor directly to the computer measurement system.

Typical sensors and their outputs are presented in table 2.2.

Table 2.2. Typical sensors and their outputs

PROPERTY	SENSOR	ACTIVE/PASSIVE	OUTPUT
Temperature	Thermocouple	Passive	Voltage
	Silicon	Active	Voltage/Current
	RTD	Active	Resistance
	Thermistor	Active	Resistance
Force / Pressure	Strain Gage	Active	Resistance
	Piezoelectric	Passive	Voltage
Acceleration	Accelerometer	Active	Capacitance
Position	LVDT	Active	AC Voltage
Light Intensity	Photodiode	Passive	Current

Active sensors require an external source of excitation: RTDs, strain-gages. *Passive* (self-generating) sensors, like thermocouples and photodiodes, do not require one.

All of these sensors can be found in renewable measurement systems.

3. CONVERTERS

3.1. INTRODUCTION

In the analog measuring circuit amplifiers perform the converters functions, which amplifying and normalizing processing signals. From amplifiers parameters depends measurement system accuracy.

From operational amplifier is required:
- high amplification,
- low input offset voltages,
- low input bias currents,
- high input impedance,
- low output impedance,
- wide bandwidth,
- high CMRR factor.

Not always the amplifiers parameters meet design assumption. Where the amplifier affect to processing signal, then on the basis of amplifier parameters given in catalogue it is needed to determine amplifier processing error (measuring circuit).

3.2. BASIC CIRCUITS WITH OPERATIONAL AMPLIFIERS

Operational amplifiers are manufactured in bipolar, BiFET, CMOS, BiMOS technologies. Characteristically parameters of operational amplifiers basis types was presented in the Table 3.1.

In the processing signal technique are use three basis structures with operational amplifiers: inverting, non-inverting and differential.

3.2.1. An inverting amplifier

The basic inverting amplifier circuit is shown in Fig. 3.1. The amplifier output is the opposite phase, polarity than the input. Output signal is the inversion of the input signal.

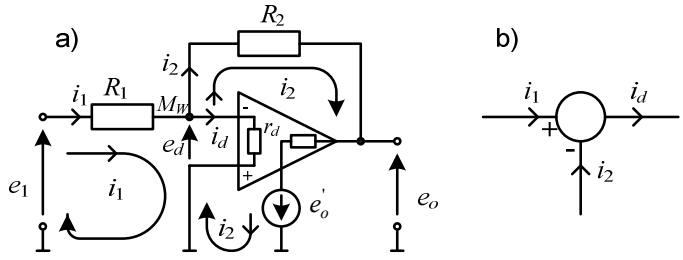
According to given in Fig. 3.1 assumptions and symbols, to the amplifier inverting terminal node influence current i_1 and currents i_2 and i_d flows out, so

$$i_1 = i_2 + i_d \,. \tag{3.1}$$

Solving the equation by nodal potential method it was obtained

$$\frac{e_1 - e_d}{R_1} = \frac{e_d - e_o}{R_2} + \frac{e_d}{r_d}, \tag{3.2}$$

where: e_d – operational amplifier input voltage,
r_d – operational amplifier differential resistance.



e_o' - is a real turn of the output voltage

Fig. 3.1. An inverting amplifier
a) connections diagram, b) summing current node

After transformation the amplifier output voltage is given

$$e_o = -\frac{R_2}{R_1}e_1 + \left(1 + \frac{R_2}{R_1} + \frac{R_2}{r_d}\right)e_d \,. \tag{3.3}$$

Taking relation into consideration describing an operational amplifier

$$e_o = -Ae_d \,, \tag{3.4}$$

where: A – amplifier gain,

Then formula (3.3) one gets

$$e_o = -\frac{R_2}{R_1}e_1 - \left(1 + \frac{R_2}{R_1} + \frac{R_2}{r_d}\right)\frac{e_o}{A} \,. \tag{3.5}$$

The second part of above relation can be regarded as a processing error. If the amplifier gain A $\to \infty$, the expression (3.5) takes the form

$$e_o = -\frac{R_2}{R_1}e_1 \,. \tag{3.6}$$

The output voltage has an opposite turn than the input voltage and the amplifier processing function depends on the values of resistors R_1 and R_2.

Table 3.1. The basic characteristic parameters of four typical operational amplifiers, supplied by voltage Uzz = ± 15V

Parameter	Symbol	Standard amplifiers		Special amplifiers		
		μA 741 (bipolar)	TL 081 (FET)	OP 07A[a] (bipolar)	MAX 430 C[b] (CMOS)	AD 817 (bipolar) fast
Differential gain	A	10^5	$2 \cdot 10^5$	$5 \cdot 10^5$	$3 \cdot 10^7$	$2 \cdot 10^4$
Common mode rejection ratio	CMRR	$3 \cdot 10^4$	$2 \cdot 10^4$	10^6	$1 \cdot 10^7$	$2 \cdot 10^5$
3dB cut-off frequency	f_A	10 Hz	10 Hz	2 Hz	1 Hz	10 kHz
Unity gain bandwidth	f_T	1 MHz	3 MHz	1 MHz	500 kHz	50 MHz
Slew rate	SR	0.66 V/μs	13 V/μs	0.3 V/μs	0.5 V/μs	350 V/μs
Differential input resistance	r_d	10^6 Ω	10^{12} Ω	$6 \cdot 10^7$ Ω	10^{12} Ω	$0.3 \cdot 10^6$ Ω
Common mode input resistance	r_s	10^9 Ω	10^{14} Ω	$2 \cdot 10^{11}$ Ω	10^{15} Ω	-
Input bias current	I_B	500 nA	200 pA	4 nA	30 pA	3 μA
Input offset current	I_{os}	100 nA	50 pA	0.1 nA	6 pA	25 nA
Input offset voltage	V_{os}	1 mV	5 mV	10 μV	2 μV	0.5 mV
Input offset current drift	$\Delta I_{os}/\Delta T$	1 nA/K	- [c]	0.1 nA/K	- [c]	0.3 nA/K
Input offset voltage drift	$\Delta V_{os}/\Delta T$	6 μV/K	10 μV/K	0.1 μV/K	0.02 μV/K	10 μV/K
Supply voltage rejection ratio	SVRR	15 μV/V	50 μV/V	3 μV/V	1 μV/V	50 μV/V
Maximum common mode voltage	$U_{s\max}$	± 13 V	+ 14.5 V - 12 V	± 14 V	+ 11 V - 15 V	+ 14.3 V - 13.1 V
Maximum output voltage	$U_{o\max}$	± 13 V	± 13 V	± 13 V	± 15 V	± 13.7 V
Maximum output current	$I_{o\max}$	± 20 mA	± 20 mA	± 20 mA	± 10 mA	± 50 mA
Input resistance	r_o	1 kΩ	100 Ω	60 Ω	1.5 kΩ	8 Ω
Supply current	I_{zz}	1.7 mA	1.4 mA	2.5mA	1 mA	7 mA

a) symmetrical amplifier in the final stage of production,
b) amplifier with an internal correction of the input offset voltage,
c) in the catalogues are not given because of the exponential factor variation

In the inverting amplifiers voltage on the inverting terminal is equal to e_d voltage (excepted polarization currents). The value of this voltage according to the table 1.1 and equation (3.4) is very small, a microvolts order, and even fragments of microvolts, and crucially depends on the amplifier gain A. Thus, the potential of the inverting input has the potential close to ground potential and it is said that at this point we have an apparent ground, also called virtual ground. This point in Fig. 3.1 is marked with letters M_W. This is a very important feature of inverting

amplifiers used in many operating circuits. The appearance of virtual ground can be explained by the existence of the amplifier summing input current node (Fig. 3.1b), where currents i_1 and i_2 influence. Current i_1 is forced by the voltage source e_1, the current i_2 is forced by the amplifier output voltage e_o. The voltage turn is consistent with the real turn of tension in the circuit. Current i_2 flows through the ground, operational amplifier input with a resistance r_d, resistor R_2, and returns to a voltage source $e_o^{'}$. In the created currents summing node the currents difference is given by

$$i_d = i_1 - i_2 \,. \tag{3.7}$$

Because the current i_d is very small in comparison with the currents i_1 and i_2 which are flowing through the amplifier input circuit, so we can assume that there is a current i_1 compensation by the current i_2, and more specifically formulated, incomplete current i_1 compensation. From the phenomenon of incomplete current compensation follows that at this node voltage drop (e_d) tends to zero and thus the node resistance also tends to zero. Thus, the amplifier input resistance seen from the voltage source e_1 is almost equal to resistance R_1. It also follows from formula (3.6) that if

$R_2 > R_1$, the signal amplification exist,
$R_2 = R_1$, Signal is inverted (gain -1),
$R_2 < R_1$, the circuit decrease (attenuate) input voltage.

3.2.2. A non-inverting amplifier

The basic non-inverting amplifier circuit is shown in Fig. 3.2. The amplifier is characterized in, that the output is the same polarity, phase as the input signal.

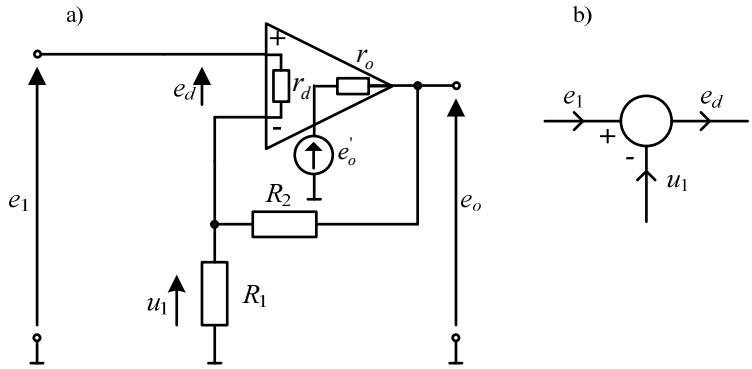


Fig. 3.2. A non-inverting amplifier
a) connections diagram b) summing voltage node

Input circuit is described by relation

$$e_1 = e_d + u_1 . \tag{3.8}$$

Because the resistor R_1 of feedback circuit has a much lower value than the amplifier input resistance r_d , so

$$e_o = \left(1 + \frac{R_2}{R_1}\right) e_1 - \left(1 + \frac{R_2}{R_1}\right) e_d . \tag{3.9}$$

Taking relation (3.1) into consideration, one gets

$$e_o = \left(1 + \frac{R_2}{R_1}\right) e_1 - \left(1 + \frac{R_2}{R_1}\right) \frac{e_o}{A} . \tag{3.10}$$

The second part of above relation can be regarded as a processing error. If the amplifier gain A $\rightarrow \infty$, then

$$e_o = \left(1 + \frac{R_2}{R_1}\right) e_1 . \tag{3.11}$$

This equation indicates that the shown amplifier configuration allows for greater than gain equal one. From the equation (3.8) follows that the operational amplifier input creates summing node e_1 i u_1 voltages, that in this node is compensation (incomplete) e_1 voltage to u_1 voltage. From the properties of the summing voltage node follows that the junction input resistance, for the accepted amplifier model, tends to infinity. Thus, e_1 voltage source "sees" the amplifier input resistance with a very high value.

3.2.3. A voltage follower

It is an amplifier with gain equal one (Fig. 3.3).

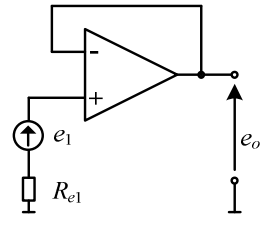


Fig. 3.3. A voltage follower

In this amplifier is 100% negative feedback, because $R_1 = \infty$ (Fig. 3.2). Output voltage, is described

$$e_o = e_1 - e_d . \tag{3.12}$$

Because $e_d << e_1$, so

$$e_o = e_1 . \tag{3.13}$$

A voltage follower is called an impedance transformer. The high impedance (resistance) voltage source e_1 coupled to non-inverting input is "seen" from the output terminal as the voltage source at value $e_o = e_1$ and a low impedance (resistance) of a few milliohms.

3.2.4. A differential amplifier

Basic structure of differential amplifier, which allows subtracting signals is presented in Fig. 3.4

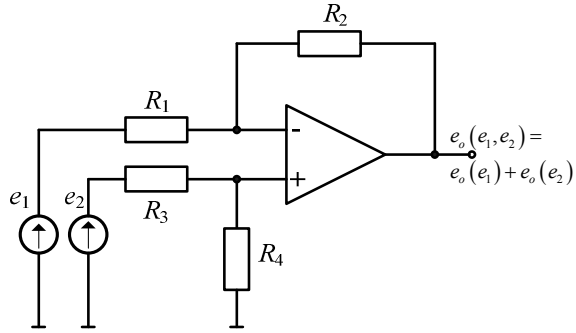


Fig. 3.4. A differential amplifier

Output voltage e_o dependence against input voltages e_1 and e_2 determined according to the superposition principle, in accordance with shown in Fig. 3.5a and 3.5b circuits.

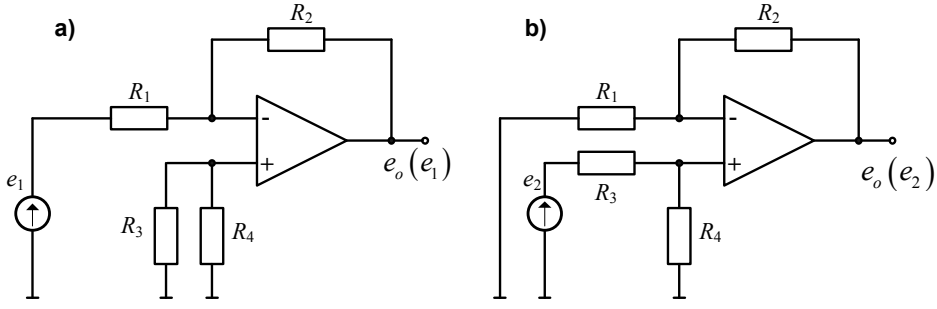


Fig. 3.5. A differential amplifier amplifying
a) e_1 voltage, b) e_2 voltage

Voltage $e_o(e_1)$ on the amplifier output shown in Fig. 3.5a, inverting configuration working, one gets

$$e_o(e_1) = -\frac{R_2}{R_1} e_1, \tag{3.14}$$

however, voltage $e_o(e_2)$ on the amplifier output shown in Fig. 3.5b, is equal

$$e_o(e_2) = \left(1 + \frac{R_2}{R_1}\right) \frac{R_4}{R_3 + R_4} e_2 . \tag{3.15}$$

Hence, the resultant voltage

$$e_o(e_1, e_2) = e_o(e_1 + e_2) = \frac{R_4}{R_1} \frac{R_1 + R_2}{R_3 + R_4} e_2 - \frac{R_2}{R_1} e_1 . \tag{3.16}$$

The fundamental disadvantage of this amplifier configuration are small values input resistances. When the condition

$$R_1 = R_3, R_2 = R_4 , \tag{3.17}$$

is carried out, then amplifier input resistance "saw" from the voltage source e_1, one gets

$$R_{in1} = R_1 \frac{1}{1 - \frac{e_2}{e_1} \frac{R_2}{R_1 + R_2}}, \tag{3.18}$$

however from the voltage source e_2 is equal

$$R_{in2} = R_1 + R_2 . \tag{3.19}$$

Where the voltages e_1 and e_1 are both equal, then

$$R_{in1} = R_{in2} = R_1 + R_2 . \tag{3.20}$$

3.3. PROPERTIES OF AMPLIFYING CIRCUITS WITH OPERATIONAL AMPLIFIERS

In the previous chapter, by way of introduction, the analysis of primary circuits in which the operational amplifiers have ideal properties, except finite values of gain and the differential input resistance [4].

Amplifying circuits are described using the static parameters relating to the *dc* and low frequency signals, moreover to dynamic parameters describing the process of high-frequency signal processing, relatively with high rate value.

Static parameters of amplifying circuits describes:

- differential gain (open loop gain) $A(0)$,
- Input offset voltage V_{os},
- input bias currents I_{B1}, I_{B2},
- input offset current I_{os},
- input offset voltage and current drift (tepearure and time),
- low frequency common mode rejection ratio CMRR ($f \approx 0$),
- low frequency noise factor F.

Dynamic parameters of amplifying circuits are:

- amplifier differential gain $A(f)$,
- 3dB cut-off frequency f_A,
- unity gain bandwidth f_T,
- slew rate SR,
- common mode rejection ratio CMRR (f),
- noise factor F.

At the next chapters the influence of presented operational amplifiers parameters on amplifying circuits properties was analyzed.

3.3.1. The input offset voltage and the offset current of operational amplifiers

Consider an operational amplifier, which properties also depend on the input offset voltage and current. Such operational amplifier equivalent circuit is shown in Fig. 3.6, it consists of an ideal amplifier and modeled sources, the source voltage V_{os} characterized by input offset voltage and current sources I_{B1} and I_{B2} representing the bias currents.

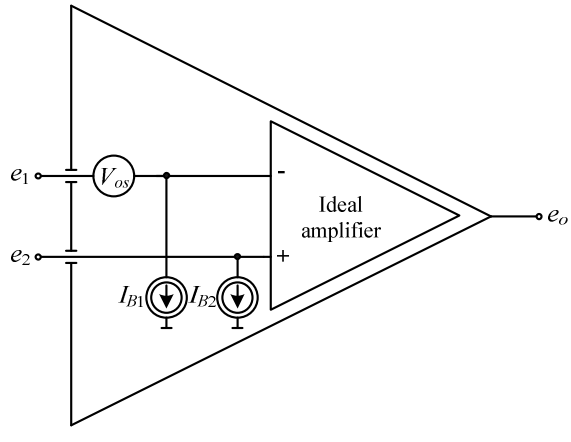


Fig. 3.6. An amplifier, which contains the input offset voltage V_{os} and the bias currents I_{B1} and I_{B2}

Listed parameters in an ideal operational amplifier are equal to zero. In the real operational amplifier the cause of input offset voltage V_{os} and the difference between bias currents I_{B1}, I_{B2} is the operational amplifier asymmetry of the input circuit formed by the differential amplifier. For example, consider a differential amplifier built from *npn* bipolar transistors, which is shown in Fig. 3.7.

Bias currents I_{B1} and I_{B2} are necessary to determine the operating points of transistors. Bias currents values depend on the transistors technology and circuit solutions of the differential amplifiers.

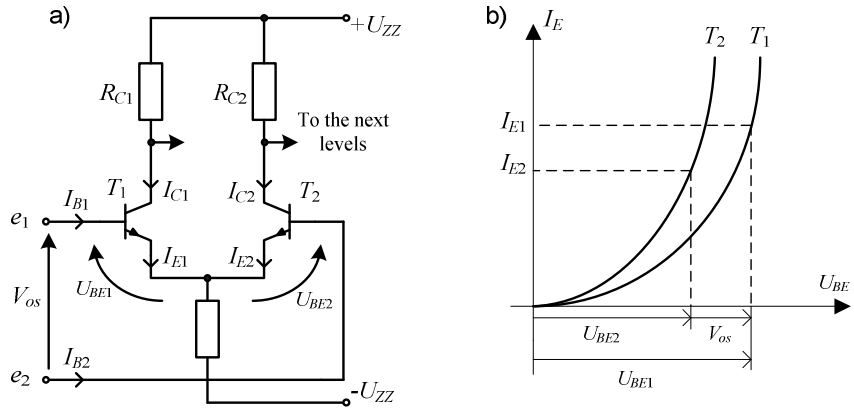


Fig. 3.7. An explanation of the causes of the input offset voltage V_{os} and occurrence of the bias currents I_{B1} and I_{B2}
a) differential circuit with bipolar transistors, b) transistors *BE* junctions characteristics

Input offset current is defined

$$I_{os} = I_{B1} - I_{B2}\,. \tag{3.21}$$

Input offset voltage, according to Fig. 3.7, is described by relation

$$V_{os} = U_{BE1} - U_{BE2}\,. \tag{3.22}$$

3.3.2. Determine the effect of the input offset voltage and the bias currents for the amplifier output voltage

Input offset voltage V_{os} and different bias currents I_{B1} and I_{B2} causes the amplifier output is a voltage which distorting signal processing [1]. Voltage calculations were performed for inverting amplifier shown in Fig. 3.8. The circuit includes input offset voltage V_{os} and the bias currents I_{B1} and I_{B2}.

Because the analyzed circuit is linear, the effect of voltage V_{os} and currents I_{B1} and I_{B2} on the output voltage e_o was determined by superposition method.

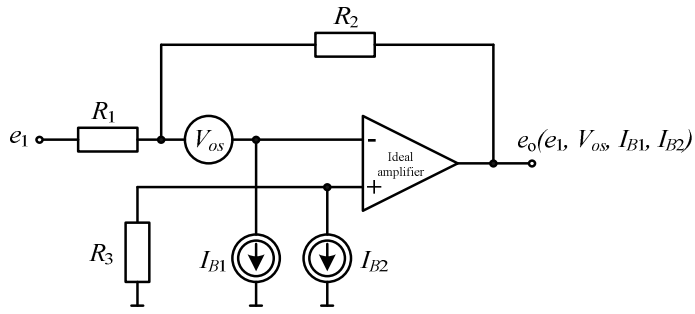


Fig. 3.8. An inverting amplifier with voltage V_{os} and currents I_{B1} and I_{B2} distorting signal processing

Output voltage in the linear circuit shown in Fig. 3.8 is described

$$e_o = f\left(e_1, V_{os}, I_{B1}, I_{B2}\right) = e_o\left(e_1\right) + e_o\left(V_{os}\right) + e_o\left(I_{B1}\right) + e_o\left(I_{B2}\right). \qquad (3.23)$$

Three last components of output voltage, occurs in relation (3.23), represents distorting voltages.

Determination of the relation between input signal e_1 and output signal $e_o(e_1)$. The relation calculated in chapter 3.2.1.

$$e_o\left(e_1\right) = -\frac{R_2}{R_1} e_1 . \qquad (3.24)$$

Determination of the input offset voltage V_{os} effect at the amplifier output voltage $e_o(V_{os})$.

We follow the superposition method. Draw a system in which the input is a source of voltage V_{os} (Fig. 3.9). We do not know the voltage V_{os} polarities and accept it arbitrarily.

Fig. 3.9.b., taking the properties of the operational amplifier, that the voltage source V_{os} of the inverting terminal can be shifted into the circuit at the non-inverting input, one gets (Chapter 3.2.2)

$$e_o\left(V_{os}\right) = \left(1 + \frac{R_2}{R_1}\right) V_{os} . \qquad (3.25)$$

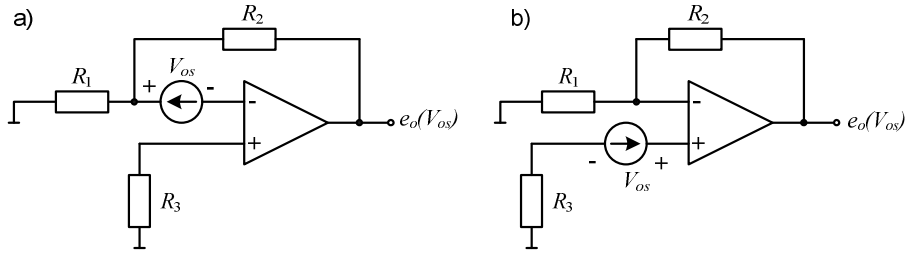


Fig. 3.9. An inverting amplifier with disturbing voltage V_{os}
a) a basic circuit, b) a modified circuit

Determination of the bias current I_{B1} effect at the amplifier output voltage $e_o(I_{B1})$.

Fig. 3.10a shows the inverting amplifier with modeled bias current source I_{B1}, and in Fig. 3.10b the modification, which uses the virtual ground M_W presence.

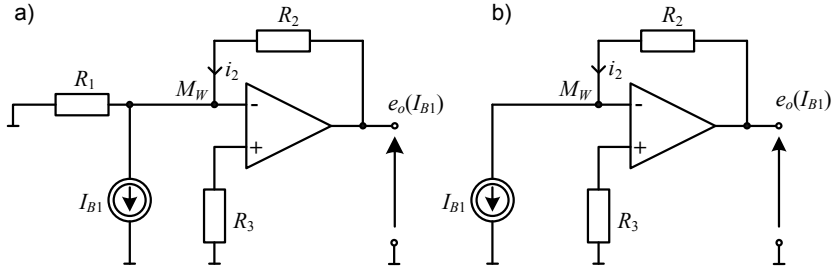


Fig. 3.10. An inverting amplifier with distorting current I_{B1}
a) a basic circuit, b) a modified circuit

Resistor R_1in Fig. 3.10b is omitted, because through this resistor does not flow current and a difference of the potential on the resistor is close to zero (equal to e_d). Therefore, it can be written, that

$$I_{B1} = i_2 = \frac{e_o(I_{B1})}{R_2}. \tag{3.26}$$

Hence

$$e_o(I_{B1}) = R_2 I_{B1}. \tag{3.27}$$

Determination of the bias current I_{B2} effect at the amplifier output voltage $e_o(I_{B2})$.

Fig. 3.11 presents the analyzed amplifier stimulated from the bias current source I_{B2}.

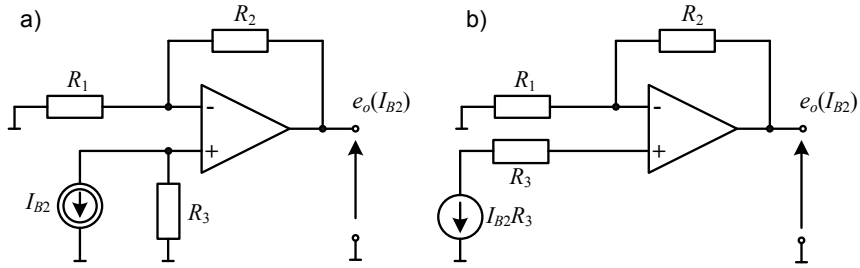


Fig. 3.11. An inverting amplifier with distorting current I_{B2}
a) a basic circuit, b) a modified circuit

Amplifier output voltage shown in Fig. 3.11b, one gets

$$e_o(I_{B2}) = -\left(1+\frac{R_2}{R_1}\right)R_3 I_{B2}\,. \tag{3.28}$$

By summing the obtained voltages, the resultant voltage on the inverting amplifier output gets

$$e_o = -\frac{R_2}{R_1}e_1 + \left(1+\frac{R_2}{R_1}\right)V_{os} + R_2 I_{B1} - \left(1+\frac{R_2}{R_1}\right)R_3 I_{B2}\,. \tag{3.29}$$

Similar considerations for the non-inverting amplifier give expression

$$e_o = \left(1+\frac{R_2}{R_1}\right)e_1 + \left(1+\frac{R_2}{R_1}\right)V_{os} + R_2 I_{B1} - \left(1+\frac{R_2}{R_1}\right)R_3 I_{B2}\,. \tag{3.30}$$

The above two equations are presented in the form

$$e_o = \begin{bmatrix}\text{output signal}\\ \text{of an ideal}\\ \text{amplifier}\end{bmatrix} + \left(1+\frac{R_2}{R_1}\right)V_{os} + R_2 I_{B1} - \left(1+\frac{R_2}{R_1}\right)R_3 I_{B2}\,. \tag{3.31}$$

This unified relation defines output voltages of two basic non-inverting and inverting amplifiers in the presence of distortions. Distortion voltages and currents V_{os}, I_{B1}, I_{B2} give the output offset voltage effect.

The formula (3.31) also indicates:

- able to the output offset voltage minimize,
- operational amplifiers nulling procedure.

Acceptable values of voltage V_{os}, bias currents I_{B1} and I_{B2} are given in the catalogs, but we do not know the polarity and voltage V_{os} value, however the currents I_{B1} and I_{B2} have similar values and flow in the same direction.

Given the bias current properties can be minimized their impact on the output offset voltage. Let us write the last two components of expression (3.31), and compare them to zero

$$R_2 I_{B1} - \left(1 + \frac{R_2}{R_1}\right) R_3 I_{B2} = 0 . \tag{3.32}$$

Assuming that currents I_{B1} and I_{B2} are equal, we obtain an expression determining the optimal value of the resistor R_3, from the viewpoint of minimizing the effects of bias currents

$$R_3 = \frac{R_1 R_2}{R_1 + R_2} . \tag{3.33}$$

If we choose the resistor R_3 according to the above relation, and currents $I_{B1} \neq I_{B2}$ then the unified equation (3.31) takes the form

$$e_o = \begin{bmatrix} \text{output signal} \\ \text{of an ideal} \\ \text{amplifier} \end{bmatrix} + \left(1 + \frac{R_2}{R_1}\right) V_{os} + R_2 I_{os} , \tag{3.34}$$

where: I_{os} - input offset current, $I_{os} = I_{B1} - I_{B2}$.

If we are operating the terms: input offset voltage V_{os} and input offset current I_{os}, then the real operational amplifier in complying with the expression (3.33) is a circuit illustrated in Fig. 3.12.

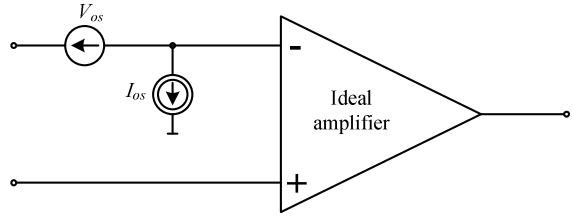


Fig. 3.12. An operational amplifier with the input offset voltage and the offset current assuming condition (3.33)

Input offset voltage V_{os} and current I_{os} depend on asymmetry of made operational amplifier. If the amplifier analysis we consider changes quantities listed above, depending on temperature changes, time and voltage fluctuations, we obtain respectively

$$V_{os}^{'} = V_{os} + \frac{\Delta V_{os}}{\Delta T}\Delta T + \frac{\Delta V_{os}}{\Delta t}\Delta t + \frac{\Delta V_{os}}{\Delta U_{ZZ}}\Delta U_{ZZ} , \tag{3.35}$$

$$I_{os}^{'} = I_{os} + \frac{\Delta I_{os}}{\Delta T}\Delta T + \frac{\Delta I_{os}}{\Delta t}\Delta t\,, \tag{3.36}$$

where: ΔT – temperature changes,
Δt – time interval,
ΔU_{ZZ} – supply voltage fluctuations.

Having substituted relations (3.35) and (3.36) into expression (3.34) and after simple transformation the following was obtained

$$e_o = \begin{bmatrix}\text{output signal}\\ \text{of an ideal}\\ \text{amplifier}\end{bmatrix} + \left(1 + \frac{R_2}{R_1}\right)V_{os}^{'} + R_2 I_{os}^{'} \tag{3.37}$$

This relation is correct, assuming that the parameters of resistors R_1, R_2 and R_3, are independent of temperature and are constant over the time.

Failure to comply with the condition $R_3 = R_1 \| R_2$ also causes an increase of the amplifier. It has been shown experimentally, that for a typical amplifiers the takes the values shown in the table. 3.2 [2]

Table 3.2. Zero drift of operational amplifiers μA 741 and TL 081 for variable values of resistor R_1 [2]

Parameter	Amplifier μA 741 bipolar	Amplifier TL 081 Bi - FET
Input offset voltage drift $\Delta V_{os}/\Delta T$	6 μV/K	10 μV/K
Input offset current drift $\Delta I_{os}/\Delta T$	1 nA/K	2 pA/K (for T = 296 K)
Differential input resistance r_d	1· 106Ω	1 · 1012Ω
Input offset voltage V_{os}	1 mV	5 mV
Input offset current I_{os}	100 nA	50 pA
Bias current I_B	500 nA	200 pA
Amplifier zero crawling in inverting Or non-inverting configuration for R_2 = 100 kΩ, R_3 = 1 kΩ		
R_1 = 1 kΩ	7 μV/K	10 μV/K
R_1 = 10 kΩ	28 μV/K	11 μV/K
R_1 = 100 kΩ	210 μV/K	18 μV/K
R_1 = 1 MΩ	2000 μV/K	80 μV/K

The results in Table 3.1 indicates, that the smallest value is obtained when the condition $R_3 = R_1 \| R_2$ is kept. When this condition is not kept then there are a high zero crawling changes occur in the amplifier μA 741 and they are caused by high

values of bias currents of the amplifier. It is assumed that the amplifier μA 741 resistors R_1, R_2 and R_3 should not exceed 10 kΩ, and in the amplifier TL 081 should be less than 100 kΩ.

3.3.3 A circuit with operational amplifiers nulling

The purpose of circuits with operational amplifiers nulling is to reduce the output offset voltage to zero value. Output offset voltage depends on the input offset voltage and input offset current caused by the asymmetry parameters of the differential amplifier (chapter 3.2.4). The effect of input offset voltage is minimized, if the voltage it will be compensated by a voltage source with the required voltage stability, integrated into the amplifier input circuit. The effect results of bias currents will be minimized when the current value of the bias currents difference is delivered into the amplifier input circuit from an auxiliary current source, characterized by an appropriate current stability. The answer to the question of whether to apply the nulling circuit with a voltage source or current source, or both at the same time, it will receive for inverting and non-inverting amplifiers consideration from equation (3.31).

In case when the amplifier is analyzed in a different configuration, it must derive formulas determining the effect of input offset voltage and bias currents to the amplifier output voltage. These formulas allow the correct selection of the operational amplifier or op-amps, and then indicate which of the nulling circuits should be applied.

The choice of output offset voltage nulling circuit and nulling technique is shown in three examples.

Example 1

In the inverting amplifier built on the operational amplifier TL 081 shown in Fig. 3.13 we should:

– choose value of resistor R_3,

– calculate the output voltage e_o (e_1, V_{os}, I_{B1}, I_{B2}),

– design the effects of input offset voltage and bias current minimize circuit.

The output offset voltage minimum value caused by bias currents after the condition (3.29) obtained

$$R_3 = \frac{R_1 R_2}{R_1 + R_2} = \frac{10 \cdot 10^3 \cdot 10 \cdot 10^3}{10 \cdot 10^2 + 10 \cdot 10^3} = 5\,\text{k}\Omega\,.$$

Amplifier output voltage describes (3.34)

$$e_o\left(e_1, V_{os}, I_{os}\right) = -\frac{R_2}{R_1} e_1 + \left(1 + \frac{R_2}{R_1}\right) V_{os} + R_2 I_{os}\,.$$

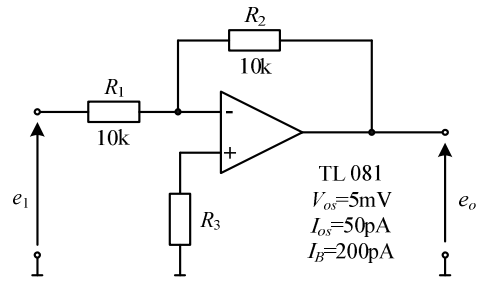


Fig. 3.13. An inverting amplifier with the operational amplifier TL 081

After substitude values

$$e_o(e_1, V_{os}, I_{os}) = -\frac{10}{10}1 + \left(1 + \frac{10}{10}\right) \cdot 5 \cdot 10^{-3} + 50 \cdot 10^{-12} \cdot 10 \cdot 10^{3},$$

calculations and admission that the output signal caused by input voltage e_1 is 100%, one gets

$$e_o(e_1, V_{os}, I_{os}) = \left(\underbrace{-1}_{100\%} + \underbrace{10 \cdot 10^{-3}}_{1\%} + \underbrace{0.5 \cdot 10^{-6}}_{0.05 \cdot 10^{-3}\%} \right) \text{V}.$$

Obtained result indicates that a significant effect on the amplifier output voltage is the input offset voltage V_{os}. Thus, the circuit which can this component minimize must be built, so must be designed the circuit to nulling input offset voltage. Sample solution of such circuit is shown in Fig. 3.14.

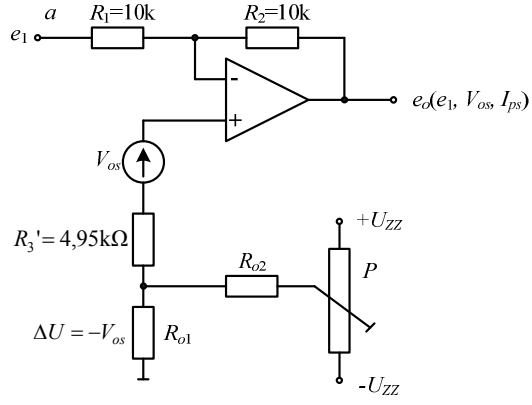


Fig. 3.14. The input offset voltage V_{os} nulling circuit

Voltage $\Delta U = -V_{os}$ was obtained from the circuit created by the stabilized voltage sources $+U_{ZZ}$ and $-U_{ZZ}$, multi-turn potentiometer P, and a resistance voltage divider R_{o1},R_{o2}. Admit resistor value R_{o1} = 50 Ω. The value of resistor R_3

determined from the condition $R_{o1}+R'_3 = R_3 = 5\ \text{k}\Omega$. However R_{o2} resistor value is calculated assuming that the voltage on the resistor R_{o1} will change in the range of $\pm\Delta U_{\max} = \pm 1{,}5\ V_{os}$.

Resistance divider output voltage is

$$\pm \Delta U_{\max} = \frac{R_{o1}}{R_{o1} + R_{o2}} \left(\pm U_{ZZ}\right).$$

Because $R_{o2} >> R_{o1}$ ten the above formula is tranformed into

$$R_{o2} = R_{o1} \frac{\pm U_{ZZ}}{\pm \Delta U_{\max}} = R_{o1} \frac{\pm U_{ZZ}}{\pm 1{,}5 V_{os}} = 50 \cdot \frac{\pm 15}{\pm 1{,}5 \cdot 5 \cdot 10^{-3}} = 100\,\text{k}\Omega\,.$$

During amplifier nulling - minimize the V_{os} component – the resistor R_1terminal *a* connects to the circuit ground and add to the amplifier output the millivoltmeter and brings its indication to zero value by changing the potentiometer *P* slider position.

ΔU voltage should be characterized by adequate stability, greater stability than the input offset voltage V_{os} determined by the temperature and time zero drift amplifier.

Example 2

For non-inverting amplifier woth operational amplifier μA 741 (Fig. 3.15) we should:

– Calculate amplifier output voltage e_o (e_1, V_{os}, I_{B1}, I_{B2}),
– design the output offset voltage minimize circuit.

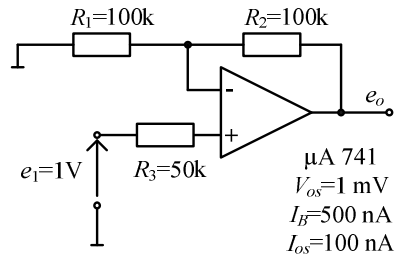


Fig. 3.15. A non-inverting amplifier with the operational amplifier μA 741

Amplifier output voltage

$$e_o\left(e_1, V_{os}, I_{B1}, I_{B2}\right) = \left(1 + \frac{R_2}{R_1}\right) e_1 + \left(1 + \frac{R_2}{R_1}\right) V_{os} + R_2 I_{B1} - \left(1 + \frac{R_2}{R_1}\right) \cdot R_3 I_{B2}$$

Because $R_3 = \dfrac{R_1 R_2}{R_1 + R_2}$

$$e_o\left(e_1, V_{os}, I_{B1}\right) = \left(1 + \frac{R_2}{R_1}\right) e_1 + \left(1 + \frac{R_2}{R_1}\right) V_{os} + R_2 I_{os}.$$

After substitude numeral values

$$e_o\left(e_1, V_{os}, I_{B1}\right) = \left(1 + \frac{100}{100}\right) 1 + \left(1 + \frac{100}{100}\right) 1 \cdot 10^{-3} + 100 \cdot 10^{3} \cdot 100 \cdot 10^{-9}$$

and calculations and admission that the output signal caused by input voltage e_1 is 100%, one gets

$$e_o\left(e_1, V_{os}, I_{B1}\right) = \left(\underbrace{2}_{100\%} + \underbrace{2 \cdot 10^{-3}}_{0.1\%} + \underbrace{10 \cdot 10^{-3}}_{0.5\%} \right) \mathrm{V}.$$

At the amplifier output are distorting voltages with the dominant voltage component caused by bias current I_{B1}. It is 0.5% compared to the amplified input signal. This distorting component can be minimized by using the circuit shown in Fig. 3.16. Bias current $I_{B1}=\Delta I$ is delivered to operational amplifier from an auxiliary current source built from the source voltages $+U_{ZZ}$, $-U_{ZZ}$, multi-turn potentiometer P and high value resistor R.

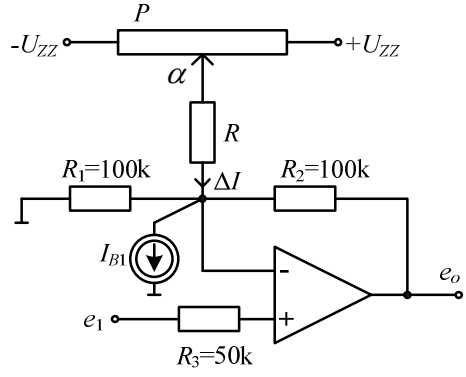


Fig. 3.16. The amplifier circuit to nulling the effects of bias current I_{B1}

Resistor R value is described

$$R = \frac{\pm U_{ZZ}}{I_B} = \frac{\pm 15\mathrm{V}}{500 \cdot 10^{-9}} = 30 \cdot 10^{6}\,\Omega$$

The operational amplifier nulling process is as follows. After the short-circuit of non-inverting input terminal to ground, multi-turn potentiometer *P* we bring the amplifier output voltage to zero (fragments of mV).

The methodology of amplifiers nulling as it is shown in Examples 1 and 2 enables the amplifier voltage zero drift quantification caused by nulling components adding.

The choice of circuit structure solutions to nulling input offset voltage and current of amplifiers makes easier schemes shown in Fig. 3.17 and Fig. 3.18.

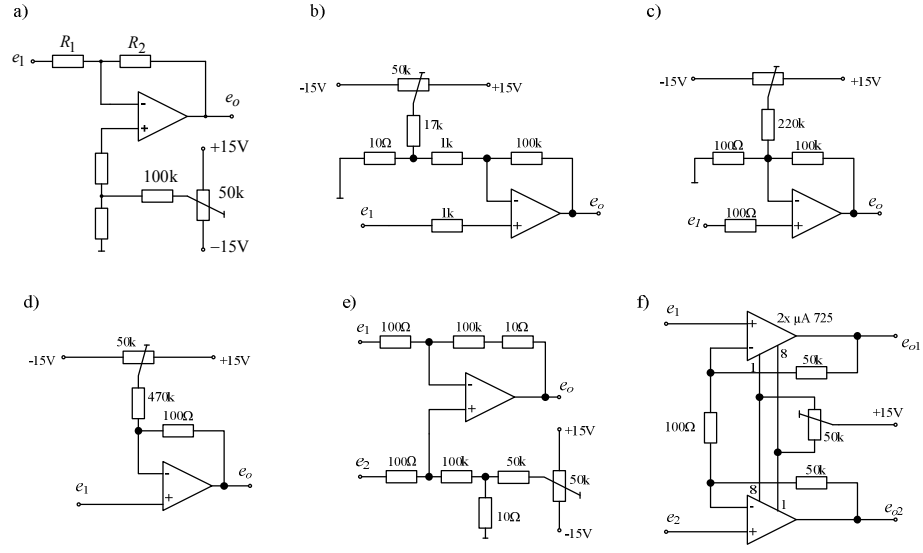


Fig. 3.17. Recommended circuits to input offset voltage nulling
a) an inverting amplifier, b), c) a non-inverting amplifier, d) a voltage follower, e), f) a differential amplifiers

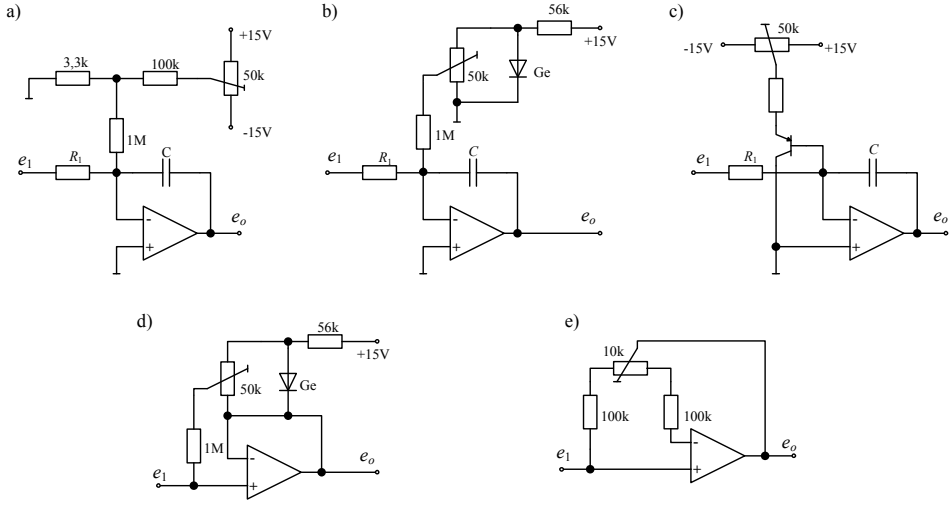


Fig. 3.18. Recommended circuits to input the offset current nulling
a), b), c) integrating circuits, d), e) voltage followers;

Common mode rejection ratio (CMRR)

Common mode rejection ratio is a realization symmetry meter of

- operational amplifiers,
- circuits with operational amplifiers, also symmetry meter,
- differential signals transmission circuits.

When the amplifier is asymmetrical, the signals linked to the inverting and non-inverting input are processed with various amplifications and there is a processing error. An analogous error occurs in a symmetrical differential signal transmission circuits.

In an ideal operational amplifier or amplifying circuit, signals amplifying tracks, seen from the inverting and non-inverting terminal, have the same gain value with opposite sign, and as we shall show, the CMRR is equal to the infinity.

We shall show also that in real circuits, the resultant amplifier $CMRR_O$ depends on:

1. amplification circuit $CMRR_{OA}$, following from operational amplifiers of CMRR.
2. Amplifying circuit structure of $CMRR_U$.
3. Tolerance of resistors used in the amplifier $CMRR_{\delta R}$.
4. Differential amplifier input impedance, common-mode and signal sources impedance $CMRR_Z$.
5. Capacity of wires connecting the signal sources to the inputs of amplifier $CMRR_C$.

Thus, the resultant $CMRR_O$ of amplifying circuit is described by function [18, 21]

$$\mathrm{CMRR}_O = f\left(\mathrm{CMRR}, \mathrm{CMRR}_{OA}, \mathrm{CMRR}_U, \mathrm{CMRR}_{\delta R}, \mathrm{CMRR}_Z, \mathrm{CMRR}_C\right).$$

Common-mode voltages are also known as summing, synphase, parallel and non-differential.

Operational amplifier CMRR

Ideal operational amplifier, show in Fig. 3.19, is described by relation

$$e_o = A\left(e_2 - e_1\right) = Ae_d, \tag{3.38}$$

where: A – amplifier voltage gain equal to differentia gain.

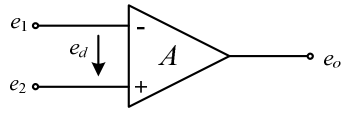


Fig. 3.19. Ideal operational amplifier with finite A gain value

If amplified signals e_1, e_2 have high and close values [2, 18], then output signal e_o of real amplifier depends not only on signal difference

$$e_d = e_2 - e_1, \tag{3.39}$$

But also depends on common-mode signals component defined

$$e_s = \frac{e_1 + e_2}{2}. \tag{3.40}$$

The Real amplifier scheme presented in Fig. 3.20.

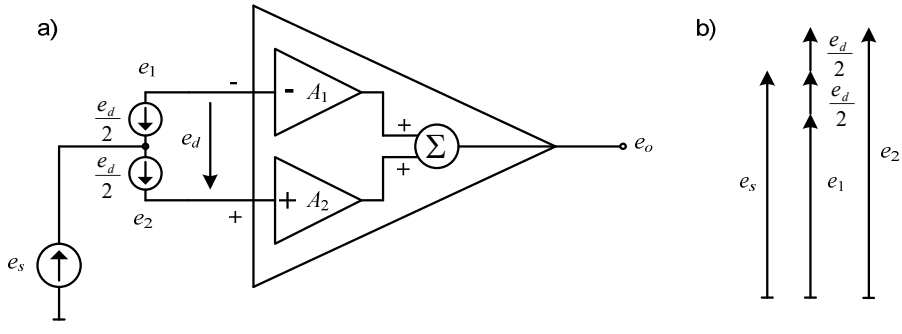


Fig. 3.20. Operational amplifiers with signals' gain tracks
a) amplifier scheme, b) amplifier output voltage interpretation

Output voltage e_o is linear combination of two input voltages e_1 i e_2

$$e_o = -A_1e_1 + A_2e_2, \tag{3.41}$$

where $A_1(A_2)$ is signal voltage gain between input – (+) and output when the input + (–) is grounded.

From the relations describing differential voltages e_d and common e_s, one gets

$$e_1 = e_s - \frac{e_d}{2}, \qquad e_2 = e_s + \frac{e_d}{2} \quad . \tag{3.42}$$

After substitude this expressions into above relation, one gets

$$e_o = \frac{A_1 + A_2}{2} e_d + \left(A_2 - A_1\right) e_s \quad . \tag{3.43}$$

Hence

$$e_o = A e_d + A_s e_s \, , \tag{3.44}$$

where differential voltage gain

$$A = \frac{A_1 + A_2}{2} \tag{3.45}$$

and common-mode voltage gain

$$A_s = A_2 - A_1 \, . \tag{3.46}$$

Taking into consideration relations (3.45) and (3.46) the expression (3.44) was obtained

$$e_o = A e_d \left(1 + \frac{A_s}{A} \frac{e_s}{e_d} \right) = A e_d \left(1 + \frac{1}{\frac{A}{A_s}} \frac{e_s}{e_d} \right) = A e_d \left(1 + \frac{1}{CMRR} \frac{e_s}{e_d} \right), \tag{3.47}$$

where:

$$\mathrm{CMRR} = \frac{A}{A_s} \tag{3.48}$$

In catalogues is presented in dB

$$\mathrm{CMRR}(\mathrm{dB}) \approx 20 \lg \frac{A}{A_s} \, . \tag{3.49}$$

According to relation (3.47) operational amplifier gain error resulting from the finite CMRR, one gets

$$\delta A_{\mathrm{CMRR}} = \frac{1}{\mathrm{CMRR}} \frac{e_s}{e_d} \tag{3.50}$$

and tends to zero when the CMRR tends to infinity.
The amplifier output voltage can be expressed by the equation

$$e_o = A\left(e_d + \frac{e_s}{\text{CMRR}}\right) = A\left(e_2 - e_1 + \frac{e_s}{\text{CMRR}}\right). \tag{3.51}$$

On the basis of this relation it can build a scheme with an ideal operational amplifier, which included the CMRR for differential signal processing error.

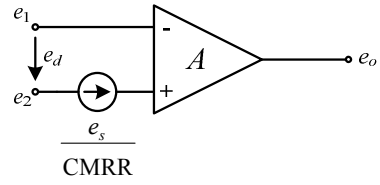


Fig. 3.21. Common-mode voltage e_s effect on differentia signal processing error

Basic amplifying structures CMRR$_{OA}$

Differential amplifier

Consider the operational amplifier CMRR effect on the differential amplifier properties with symmetrically matched resistors. Under this assumption, common signal attenuation effect on scheme represents the voltage source e_s/CMRR. Polarization of this source has been chosen arbitrarily.

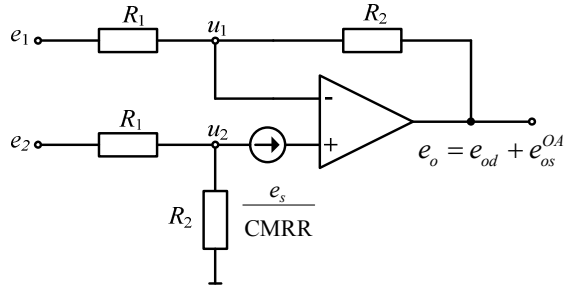


Fig.3.22. Common-mode voltage e_s effect on the processing error of differential amplifier

Differential amplifier is describing by the equations [23]

$$e_o = A\left(u_2 - u_1 + \frac{e_s}{\text{CMRR}}\right),$$

$$u_1 = e_o \frac{R_1}{R_1 + R_2} + e_1 \frac{R_2}{R_1 + R_2}, \tag{3.52}$$

$$u_2 = e_2 \frac{R_2}{R_1 + R_2}.$$

Transforming these expressions and assuming that $A\beta >> 1$, one gets

$$e_o = \frac{R_2}{R_1}(e_2 - e_1) + \frac{R_1 + R_2}{R_1}\frac{e_s}{\text{CMRR}} = e_{od} + e_{os}^{OA}, \tag{3.53}$$

where:

$$e_{od} = \frac{R_2}{R_1}(e_2 - e_1), \tag{3.54}$$

Is an output voltage caused by differential voltage $e_d = e_2 - e_1$,

$$e_{os}^{OA} = \frac{R_1 + R_2}{R}\frac{e_s}{\text{CMRR}}, \tag{3.55}$$

Is an output voltage caused by common-mode voltage e_s.

Differential gain of this amplifier

$$A_u = \frac{e_{od}}{e_d} = \frac{\frac{R_2}{R_1}(e_2 - e_1)}{e_2 - e_1} = \frac{R_2}{R_1}. \tag{3.56}$$

Differential amplifier common-mode gain

$$A_{us} = \frac{e_{os}^{OA}}{e_s} = \frac{\frac{R_1 + R_2}{R_1} \cdot \frac{e_s}{\text{CMRR}}}{e_s} = \frac{R_1 + R_2}{R_1}\frac{1}{\text{CMRR}}. \tag{3.57}$$

Hence, the differential amplifier common mode rejection ratio due to a finite value CMRR of the operational amplifier

$$\text{CMRR}_{OA} = \frac{A_u}{A_{us}} = \frac{\frac{R_2}{R_1}}{\frac{R_1 + R_2}{R_1}\frac{1}{\text{CMRR}}} = \frac{R_2}{R_1 + R_2}\text{CMRR}. \tag{3.58}$$

An equation shows that when the differential amplifier gain value increases, the CMRR_{OA} proceed to operational amplifier CMRR.

Below the output voltage e_o, described by formula (3.53), is expressed by a voltages e_1, e_2 and the CMRR.

Operational amplifier common-mode voltage

$$e_s = \frac{u_1 + u_2 + \dfrac{e_s}{\text{CMRR}}}{2}. \tag{3.59}$$

There are relations between voltages

$$u_1 \approx u_2, \qquad u_1, u_2 >> \frac{e_s}{\text{CMRR}}. \tag{3.60}$$

From above expressions obtain, that when $e_s \approx u_2$, then taking relation (3.52) into consideration, one gets

$$e_s = e_2 \frac{R_2}{R_1 + R_2}. \tag{3.61}$$

Hence the differentia amplifier output voltage

$$e_o = \frac{R_2}{R_1}(e_2 - e_1) + \frac{R_2}{R_1}\frac{e_2}{\text{CMRR}} = e_{od} + e_{os}^{OA}. \tag{3.62}$$

Differential amplifier processing error caused by the finite CMRR value of operational amplifier increases with gain increasing.

Example 3

Operational amplifier μA741 with CMRR = $3 \cdot 10^4$ was used in differentia amplifier structure. Feedback resistors R_1 = 1 kΩ and R_2 = 100 kΩ. Output voltages are equal e_1 = 9,950 V, e_2 = 10,050 V. Describe an error caused by operational amplifier CMRR finite value.

Relative error caused by CMRR finie value

$$\delta e_{os}^{OA} = \frac{e_{os}^{OA}}{e_{od}} \cdot 100 = \frac{\dfrac{R_2}{R_1}\dfrac{e_2}{\text{CMRR}}}{\dfrac{R_2}{R_1}(e_2 - e_1)} 100 = \frac{e_2}{(e_2 - e_1)\text{CMRR}} 100$$

$$\delta e_{os}^{OA} = \frac{10.050}{(10.050 - 9.950)3 \cdot 10^4} \cdot 100 = 0.33\ \%\ .$$

Processing error is 0,33 %.

Non-inverting amplifier

CMRR effect on non-inverting amplifier work (Fig. 3.23) were determined based on the superposition principle.

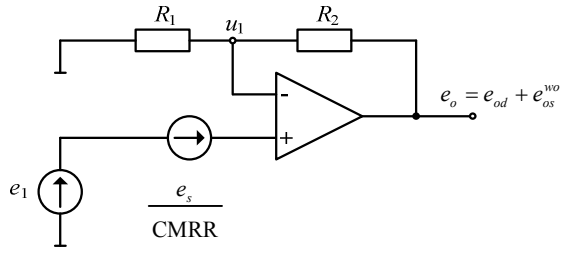


Fig. 3.23. Common-mode voltage e_s effect on non-inverting amplifier processing error

Non-inverting amplifier output voltage, after taking into account the gain A and feedback β

$$e_o = e_1\left(1+\frac{R_2}{R_1}\right)\frac{1}{1+\dfrac{1}{A\beta}}. \tag{3.63}$$

Components e_{od} and e_{os}^{OA} of voltage e_o will be determine according to superposition principle. In the first step, we assume that $e_s/\mathrm{CMRR}=0$. Then output voltages

$$e_{od} = e_1\left(1+\frac{R_2}{R_1}\right)\frac{1}{1+\dfrac{1}{A\beta}}. \tag{3.64}$$

In the second step we assume that $e_1 = 0$ and we get

$$e_{os}^{OA} = \frac{e_s}{\mathrm{CMRR}}\left(1+\frac{R_2}{R_1}\right)\frac{1}{1+\dfrac{1}{A\beta}}. \tag{3.65}$$

Amplifier resultant output voltage

$$e_o = e_{od} + e_{os}^{OA} = e_1\left(1+\frac{R_2}{R_1}\right)\frac{1}{1+\dfrac{1}{A\beta}} + \frac{e_s}{\mathrm{CMRR}}\left(1+\frac{R_2}{R_1}\right)\frac{1}{1+\dfrac{1}{A\beta}}. \tag{3.66}$$

Non-inverting amplifier differential gain

$$A_u = \frac{e_{od}}{e_1} = \left(1+\frac{R_2}{R_1}\right)\frac{1}{1+\dfrac{1}{A\beta}}, \tag{3.67}$$

get cause that the second input terminal of the analyzed amplifier creates a point connecting a resistor R_1 to ground and has the zero potential. Thus, differential voltage of non-inverting amplifier is e_1.

Non-inverting amplifier common-mode gain

$$A_{us} = \frac{e_{os}}{e_s} = \left(1 + \frac{R_2}{R_1}\right) \frac{1}{1 + \dfrac{1}{A\beta}} \cdot \frac{1}{\text{CMRR}}. \tag{3.68}$$

The non-inverting amplifier common mode rejection ratio due to a finite value CMRR of the operational amplifier

$$\text{CMRR}_{OA} = \frac{A_u}{A_{us}} = \text{CMRR}\ . \tag{3.69}$$

The relation shows that non-inverting amplifier CMRR_{OA} takes the same value as the CMRR of the operational amplifier.

If the common-mode voltage express with e_1, then

$$e_s = \frac{u_1 + e_1 + \dfrac{e_s}{\text{CMRR}}}{2} \approx e_1, \tag{3.70}$$

since

$$u_1 \approx e_1, \qquad u_1, e_1 >> \frac{e_s}{\text{CMRR}} \tag{3.71}$$

and non-inverting amplifier output voltage is equal

$$e_o = e_{od} + e_{os}^{wo} = e_1\left(1 + \frac{R_2}{R_1}\right) \frac{1}{1 + \dfrac{1}{A\beta}} + \frac{e_1}{\text{CMRR}}\left(1 + \frac{R_2}{R_1}\right) \frac{1}{1 + \dfrac{1}{A\beta}}. \tag{3.72}$$

Equation second part characterizes non-inverting amplifier processing error.

Example 4

Operational amplifier μA 741 works in non-inverting amplifier structure processing signal e_1 = 0.100 V. Feedback resistors are equal R_1 = 1 kΩ, R_2 = 99 kΩ. Amplifier catalog data $A = 10^5$ V/V, CMRR = $3 \cdot 10^4$. Calculate an amplifier processing CMRR factor.

Error caused by operational amplifier gain finite values

$$\delta A_u^A = \frac{1}{A\beta}\cdot 100 = \frac{1}{A\dfrac{R_1}{R_1+R_2}}100 = \frac{1}{10^5\dfrac{1}{1+99}}\cdot 100 = 0.1\% \ .$$

However, the error caused by operational amplifier finite CMRR value

$$\delta e_{os}^{OA} = \frac{e_{os}^{OA}}{e_o}\cdot 100 \approx \frac{e_{os}^{OA}}{e_{od}}\cdot 100 = \frac{1}{\text{CMRR}}\cdot 100 = \frac{1}{3\cdot 10^4}\cdot 100 = 0.0033\% \ .$$

The error δe_{os}^{OA} in comparison with error δA_u^A is negligibly small. The error δA_u^A can be corrected by using analytical relations or do feedback resistors calibration using specialized measurement system.

Example 5

Non-inverting amplifier with β = 0,1 need to amplify the signal e_1 = 1 V. Amplifier processing error caused by non-ideal attenuation of CMRR should be lower than 100 μV. What CMRR should be characterized by an operational amplifier? In the calculation should be assumed that. $A\beta >> 1$.

Amplifier processing error caused by operational amplifier finite CMRR value

$$e_{os}^{OA} = \frac{e_1}{\text{CMRR}}\left(1+\frac{R_2}{R_1}\right)\frac{1}{1+\dfrac{1}{A\beta}}.$$

Given that $A\beta$>>1, one gets

$$e_{os}^{OA} = \frac{e_1}{\text{CMRR}}\left(1+\frac{R_2}{R_1}\right) = \frac{e_1}{\text{CMRR}}\frac{1}{\beta} \le e_{os}^{OA'},$$

where $e_{os}^{OA'} = 100\,\mu\text{V}$ – allowable processing error value

From this inequality we obtain

$$\text{CMRR} \ge \frac{1}{\beta}\frac{e_1}{e_{os}^{OA'}} = \frac{1}{0.1}\frac{1}{100\cdot 10^{-6}} = 10^5 \ \square \ 100\,\text{dB}.$$

Amplifier OP 07 A comply this condition, which has CMRR = 10^6 □ 120 dB.

Voltage follower

The voltage follower output signal after taking into account the operational amplifier gain A finite values and CMRR determined by the formula (3.72) describing the non-inverting amplifier. Assuming that β = 1, one gets

$$e_o = e_1 \frac{1}{1+\frac{1}{A}} + \frac{e_s}{\text{CMRR}} \frac{1}{1+\frac{1}{A}} = e_{od} + e_{os}^{OA}. \tag{3.73}$$

Voltage follower differential gain

$$A_u = \frac{e_{od}}{e_1} = \frac{1}{1+\frac{1}{A}}. \tag{3.74}$$

Common-mode gain

$$A_{us} = \frac{e_{os}^{OA}}{e_s} = \frac{1}{1+\frac{1}{A}} \frac{1}{\text{CMRR}}. \tag{3.75}$$

Voltage follower CMRR

$$\text{CMRR}_{OA} = \frac{A_u}{A_{us}} = \text{CMRR}. \tag{3.76}$$

Given, that $e_s \approx e_1$ equation (3.73) can be expressed as

$$e_o = e_1 \frac{1}{1+\frac{1}{A}} \left(1 + \frac{1}{\text{CMRR}}\right) \approx e_1 \left(1 - \frac{1}{A} + \frac{1}{\text{CMRR}}\right), \tag{3.77}$$

where two last part characterizes voltage follower processing error.

Example 6

In the voltage followers was used operational amplifiers μA 741 and OP 07A. Calculate processing errors caused by operational amplifier gain A and CMRR finite value.

From catalog data

μA 741, $A = 10^5$, CMRR = 3 10^4,

OP 07A, $A = 5 \cdot 10^5$, CMRR = 10^6.

Errors caused by operational amplifiers gain finite value:
for μA 741

$$\delta A_u^A = \frac{1}{A} \cdot 100 = \frac{1}{10^5} \cdot 100 = 0{,}001\%,$$

for OP 07A

$$\delta A_u^A = \frac{1}{A} \cdot 100 = \frac{1}{5\,10^5} \cdot 100 = 0{,}0002\,\% .$$

Errors caused by non-ideal CMRR attenuation
for μA 741

$$\delta A_{os}^{OA} = \frac{1}{\mathrm{CMRR}} \cdot 100 = \frac{1}{3 \cdot 10^4} \cdot 100 = 0.0033\,\% ,$$

for OP 07A

$$\delta A_{os}^{OA} = \frac{1}{\mathrm{CMRR}} \cdot 100 = \frac{1}{10^6} \cdot 100 = 0.0001\,\% .$$

The least favorable processing errors one gets
for amplifier μA 741, $\delta e_o = 0.0043$ %, a
for amplifier OP 07A, $\delta e_o = 0.0003$ % .

Example 7 [23]
Operational amplifier with voltage gain A = 60 dB and CMRR = 60 dB, is use with open loop as a comparator. Input signal is comparing with reference voltages 1 V.

Task 1. Determine the unwanted voltage value that occurs at the output of the comparator when $e_1 = e_2 = 1$ V.
Comparation process is realized in the amplifier structure show in Fig. 3.24.
Operational amplifier output voltage

$$e_o = e_{od} + e_{os} = A\left(e_2 - e_1 + \frac{e_s}{\mathrm{CMRR}} \right).$$

Hence

$$e_{os} = A\frac{e_s}{\mathrm{CMRR}} = A\frac{e_1}{\mathrm{CMRR}} = 1 \cdot 10^3 \frac{1}{1 \cdot 10^3} = 1\,\mathrm{V} .$$

When voltages e_1=e_2, then finite values of A and CMRR causes, that on the amplifier output will be $e_{os}^{wo} = 1\,\mathrm{V}$ voltage value.

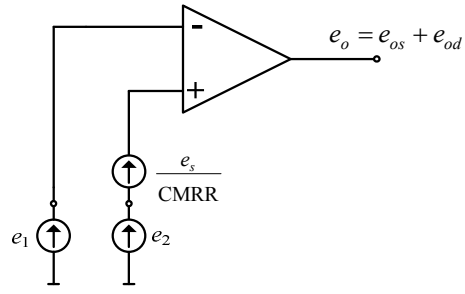


Fig. 3.24. Operational amplifier in a comparator configuration

Task 2. Determine the value of the CMRR which should have operational amplifier that the output voltage component does not exceed the voltage $e'_{os} \le 0.1V$, when voltages $e_1 = e_2 = 1$ V.

The inequality

$$e_{os} = A\frac{e_1}{\text{CMRR}} \le e'_{os},$$

shows, that amplifier CMRR should comply the relation

$$\text{CMRR} \ge A\frac{e_s}{e'_{os}} = 1\cdot 10^3 \frac{1}{0.1} = 10^4.$$

CMRR should be equal Or greater than 10^4 that is 80 dB.

3.4 INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are characterized by high input resistances and high attenuation values of CMRR. Fig. 3.25 has shown a modular input circuit of instrumentation amplifier called DIDO (Differential Input Differential Output). Manufactured instrumentation amplifiers has DIDO input structure realized by various structure means ensuring symmetry of the input circuit.

If we assume, that the amplification of the operational amplifiers A_1, $A_2 \to \infty$, and feedback amplifiers input resistances r_{wes1} and $r_{wes2} >> R_1$, R_2, R_3, then the amplifier describes equation

$$i_1 = \frac{e_A - e_B}{R_1},$$

$$e_{o1} = e_A + i\,R_2, \tag{3.78}$$

$$e_{o2} = e_B - i\,R_3.$$

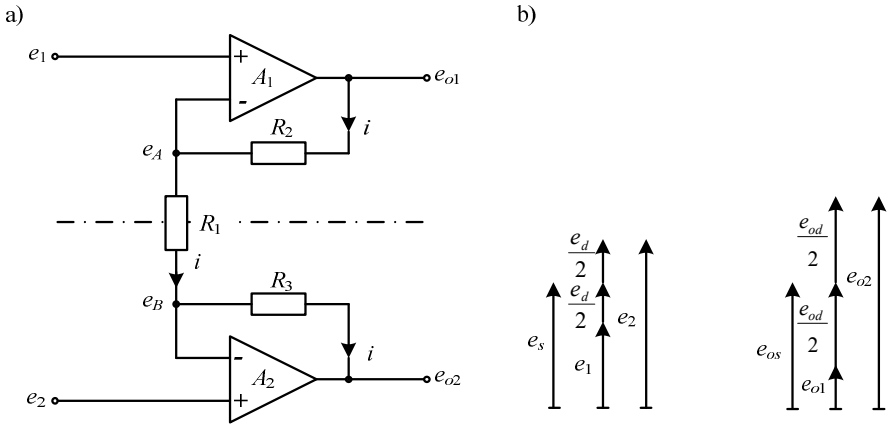


Fig. 3.25. Symmetrical amplifier with the differential input and output:
a) amplifier structure, b) amplifier input and output voltages

Given, that $e_A = e_1$, a $e_B = e_2$ then the above relations are represented by equation

$$e_{o1} = \left(1 + \frac{R_2}{R_1}\right) e_1 - \frac{R_2}{R_1} e_2 , \tag{3.79}$$

$$e_{o2} = -\frac{R_3}{R_1} e_1 + \left(1 + \frac{R_3}{R_1}\right) e_2 .$$

The amplifier difference output voltage is

$$e_{o2} - e_{o1} = \left(1 + \frac{R_2}{R_1} + \frac{R_3}{R_1}\right)\left(e_2 - e_1\right). \tag{3.80}$$

If the assumptions in the amplifier are met then signals e_1 and e_2 subject to the same processing. This equation shows, that the amplifier is symmetrical.

When we assume, that $R_2 = R_3$, then processing equation has form

$$e_{o2} - e_{o1} = \left(1 + 2\frac{R_2}{R_1}\right)\left(e_2 - e_1\right). \tag{3.81}$$

Amplifier differential gain

$$A_u = \frac{e_{o2} - e_{o1}}{e_2 - e_1} = 1 + 2\frac{R_2}{R_1} . \tag{3.82}$$

If at the amplifier inputs we will put common-mode voltage e_s, then according to the equation (3.79) at the output we will get voltages

$$e_{o1s} = \left(1 + \frac{R_2}{R_1}\right) e_s - \frac{R_2}{R_1} e_s = e_s , \tag{3.83}$$

$$e_{o2s} = -\frac{R_3}{R_1} e_s + \left(1 + \frac{R_3}{R_1}\right) e_s = e_s .$$

These equations shows that the common-mode gain of the amplifier is

$$A_{us}^U = \frac{e_{o1s}}{e_s} = \frac{e_{o2s}}{e_s} = 1 . \tag{3.84}$$

Hence, the CMRR_U depends on amplifier structure

$$\mathrm{CMRR}_U = \frac{A_u}{A_{us}^U} = 1 + 2\frac{R_2}{R_1} . \tag{3.85}$$

DIDO symmetrical amplifier characterize in very good properties, has a high input resistance, common-mode voltage gain is equal 1, and the CMRR_U factor increases with the gain.

Example 8

Instrumentation amplifier consists of a DIDO amplifier and differential amplifier (Fig. 3.26). Determine resultant common mode signal component attenuation factor, taking into account CMRR_U factor of DIDO amplifier and $\mathrm{CMRR}_{\delta R}$ factor of differential amplifier.

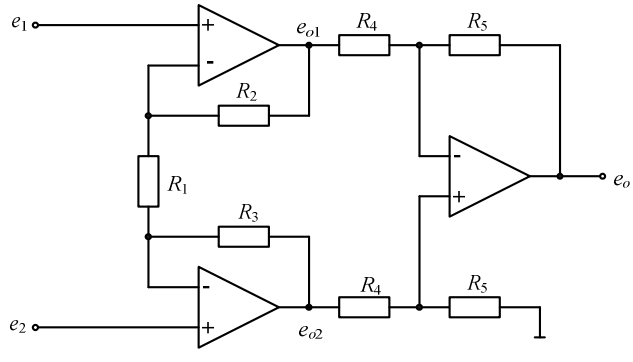


Fig. 3.26. Instrumentation amplifier formed from the DIDO amplifier and the differential amplifier.

Amplifier describe equations

$$e_{o2} - e_{o1} = \left(1 + 2\frac{R_2}{R_1}\right)(e_2 - e_1),$$

$$e_o = \frac{R_5}{R_4}(e_{o2} - e_{o1}) - \frac{R_5}{R_4 + R_5} 2\delta R\, e_{os2},$$

$$e_{os2} = e_{os1} = e_2 = e_1 = e_s.$$

Amplifier processing relation

$$e_o = \left(1 + 2\frac{R_2}{R_1}\right)\frac{R_5}{R_4}(e_2 - e_1) - \frac{R_5}{R_4 + R_5} 2\delta R\, e_s = e_{od} + e_{os}.$$

Differential gain

$$A_u^{1,2} = \frac{e_{od}}{e_2 - e_1} = \left(1 + 2\frac{R_2}{R_1}\right)\frac{R_5}{R_4}.$$

Common-mode gain

$$A_{us}^{1,2} = \frac{e_{os}}{e_s} = \frac{R_5}{R_4 + R_5} 2\delta R.$$

Resultant common mode component attenuation factor

$$\mathrm{CMRR}_o^{1,2} = \frac{A_u^{1,2}}{A_u^{1,2}} = \frac{1 + 2\frac{R_2}{R_1}}{1} \quad \frac{R_4' + R_5}{R_4} \frac{1}{2\delta R} = \mathrm{CMRR}_U^1\, \mathrm{CMRR}_{\delta R}^2.$$

In the analyzed amplifier resultant common mode component attenuation factor is a factors product of amplifier attenuation stages. This principle is fulfilled only in differential circuits.

Table 3.3. presents parameters of selected amplifiers.

Tab.3.3. Selected instrumentation amplifiers parameters , for $T = 25\ ^{o}C$

PARAMETR	Modular	Monolithic				
	3620J	INA110	INA118	AD-620	AMP-01	AMP-05
	Burr - Brown			Analog Devices		
Gain setting	1 to 10 000	1 to 500	1 to 1000	1 to 1000	0.1 to 10000	1 to 1000
Gain characteristic nonlinearity %	0.01	0.004	0.002	0.001	0.005	0.002
Offset input voltage mV	0.2	0.2	0.05	0.03	1	0.3
Bias current nA	25	0.02	1	0.5	1	0.02
Offset input voltage drift µV/oC	2	4	0.5	0.3	20	5
Offset input current drift pA/oC	200	-	40	1.5	3	-
Differential input resistance / capacity GΩ/pF	3·102	5·103//6	10//1	10//2	10	103//8
Common-mode input resistance / capacity GΩ/pF	103	2·103//1	10//4	10//2	20	-
CMRR, from DC to 60 Hz for sources of resistance 1kΩ						
$A_u = 1$	65	40	40	40	95	95
$A_u = 10$	74	104	110	110	115	105
$A_u = 100$	90	110	120	130	125	110
$A_u = 1000$ dB	100	-	125	130	125	110
Bandwidth (-3 dB) Au = 100 kHz	300	470	70	120	82	120
Slew rate V/µs	30	17	0.9	15	13	7.5
Input voltage noise from 0.1 Hz to 10 Hz, A_u=100 µVpp	1	0.1	0.11	0.28	0.16	0.16

3.5. ISOLATION AMPLIFIERS

The task of isolation amplifiers (with the isolation barrier) is galvanic input signal separation from the circuit of which is transferred amplified output signal. Separation of these circuits provides isolation barrier, which for the DC voltages and currents must be characterized by a small leakage currents and for AC voltages and currents, small capacitive currents.

Amplifiers with an isolation barrier are used in the following cases:

1. when the common-mode component of processed signal is greater than the operational amplifier supply voltage,
2. when security of people and animals against electric shock is required – e.g. patients and doctors in hospitals in the event of isolation failure in the electro-medical instruments,
3. the ground separation is required e.g. in the power electronic system the control system grounds must be separated from ground of executive system, then over-voltages and disturbances formed during commutation in executive system are not transferred to the control circuit, e.g. in industrial measurement systems grounds separation minimizes the effect of disturbances carried by the grounds on processed signals.

Specialized operational amplifiers are powered by voltage $U_{ZZ} = \pm$ 150V. When common-mode voltage e_s does not exceed 150V then the system as shown in Fig. 3.27 could be used,.

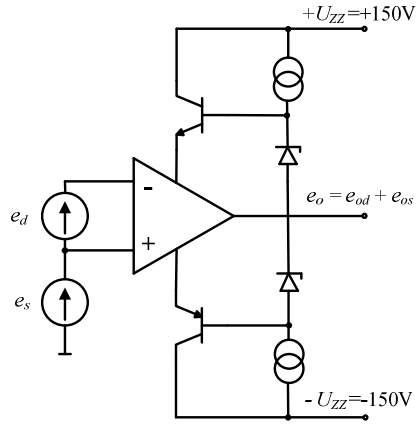


Fig. 3.27. Circuit structure of the differential signal e_d amplifying, when $e_s < |U_{ZZ} = \pm 150\,\mathrm{V}|$

The amplifier output voltage is described by the formula

$$e_o = A_u\left(e_d + \frac{e_s}{\mathrm{CMRR}}\right) = e_{od} + e_{os}\,. \tag{3.86}$$

In many cases, the measured differential voltage is applied to a much higher common-mode voltage, ranging up to several kilovolts. To overcome such a large voltage difference, measuring system should be divided into two parts separated by an amplifier isolation barrier as it is shown in Fig. 3.28.

To supply the amplifier with an isolation barrier requires two power supplies isolated from each other. Isolation of the input stage supply should have the same properties as isolation barrier.

Signals transmission through the amplifier isolation barrier is carried out with the degree of coupling:

- transformer,
- capacitance,
- optoelectronic.

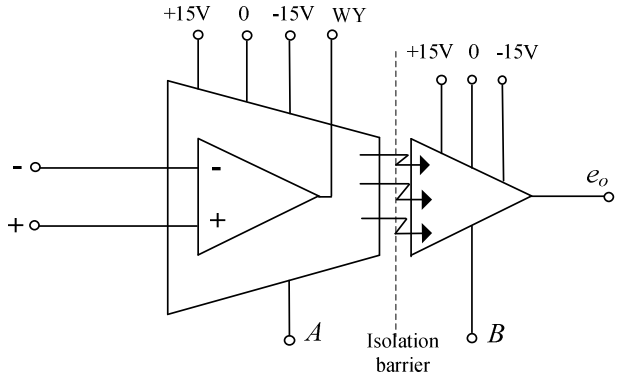


Fig. 3.28. Isolation amplifier structure,
A,B – grounds of input and output circuits

Transformer coupled amplifiers have a relatively large dimensions (e.g. AD 210 has a 25.4 x 53.3 x 8.9 mm). Into the amplifier casing is a DC/DC converter, which is powered the input stage and amplifier does not require a separated power supply with a higher isolation durability. Bandwidth may be 100kHz. Nonlinearity error of gain characteristic is below 0.005%. In the amplifier is used amplitude modulation.

Capacitance coupled amplifiers have a small size and wide bandwidth of 100 kHz. Permissible voltage on the isolation barrier is 6 kV. Have greater nonlinearity from 0.01% to 0.25%. In the amplifiers are used pulse width modulation.

Optoelectronic coupled amplifiers have a small size, low bandwidth of 5 kHz and large nonlinearity errors on the level of 0.5%.

Amplifier structure with an isolation barrier is shown in Fig. 3.29, where indicated the input differential voltage e_d ,, common-mode voltage e_s and voltage u_{is} occurring on the isolation barrier.

Amplifier output voltage depends not only on the differential voltage e_d , but it is also a function of voltages e_s and u_{is} . Isolation barrier voltage u_{is} affects the isolation amplifier input stage by the isolation barrier resistance and capacity and causes at the amplifier output disturb voltage e_{oi} . The voltage e_{oi} relation from voltage u_{is} and gain A_{ub} ($A_{ub} = 1$) of isolation amplifier determine IMRR factor (Isolation Mode Rejection Ratio) [23]

$$\text{IMRR} = \frac{A_{ub}}{\frac{e_{oi}}{u_{is}}} = \frac{1}{\frac{e_{oi}}{u_{is}}}, \tag{3.87}$$

where : A_{ub} – isolation amplifier gain $A_{ub} = 1$,

u_{is} – isolation barrier voltage,

e_{oi} – output voltage component caused by voltage u_{is}.

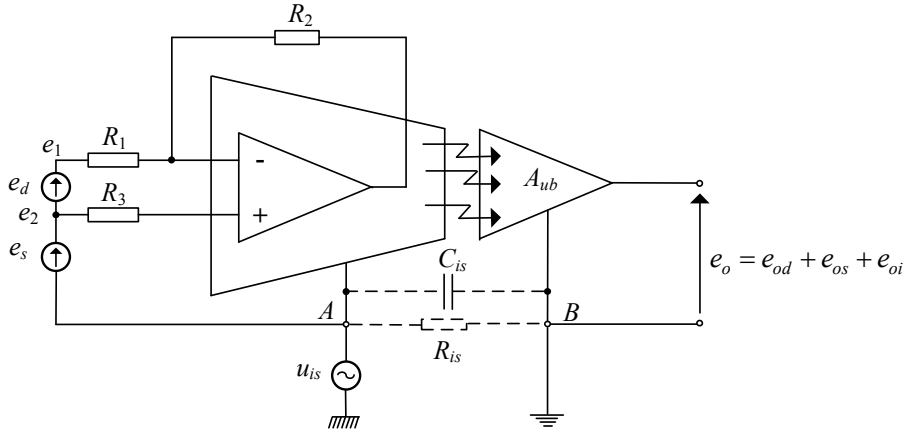


Fig. 3.29. An isolation amplifier

Amplifier output voltage depends not only on the voltage differential e_d, but it is also a function of voltages e_s and u_{is}. Voltage on the barrier of insulation u_{is} affects the input stage amplifier with an isolation barrier, through the resistance and capacity of the isolation barrier and causes the output of the amplifier voltage interfere e_{oi}. The dependence on the voltage e_{oi} and voltage u_{is} and gain A_{ub} ($A_{ub} = 1$),of amplifier with an isolation barrier, determined factor IMRR (Isolation Mode Rejection Ratio) [23]

Taking into account the effect of voltage u_{is} (IMRR ratio) and voltage e_s (CMRR ratio) at the amplifier output voltage we get

$$e_o = e_{od} + e_{os} + e_{oi} = A_u\left(e_2 - e_1 + \frac{e_s}{\text{CMRR}}\right) + \frac{u_{is}}{\text{IMRR}}. \qquad (3.88)$$

IMRR ratio is often two orders greater than the CMRR ratio. However, the voltage u_{is} effect on the processing result, compared with the voltage e_s may be more significant, because this voltage can be up to three orders higher than the voltage e_s.

The measurement of electro-medical processing signals are less than 15V ($e_s < 15\text{V}$), and the isolation barrier voltage does not exceed 1V ($u_{is} < 1\text{V}$). Due to the patients and doctors security should be used the system shown in Fig. 3.30.

In this structure, the common-mode voltage is less than the input amplifier supply voltage $e_s < |U_{ZZ} = \pm 15\,\mathrm{V}|$.

The input amplifier ground is located on the transducer ground potential and measured object ground. The output amplifier ground has measuring system ground. Between these grounds is coupling capacitance C_{is}, isolation leakage R_{is} and the potential difference u_{is}.

Because the potential difference u_{is} on the isolation barrier, caused by disturbance currents flowing through the ground, has a small value and does not exceed 1V, so output voltage component e_{oi} induced by u_{is} may be skipped and the amplifier output voltage is equal

$$e_o = A_u\left(e_d + \frac{e_s}{\mathrm{CMRR}}\right). \tag{3.89}$$

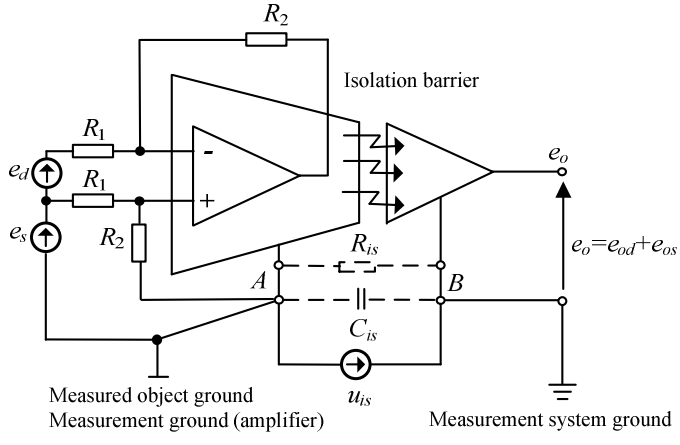


Fig. 3.30. An isolation amplifier – a sample solution $e_s \le |U_{ZZ} = \pm 15\mathrm{V}|$
- ensures safety of doctors and patients

When the common-mode voltage takes high values $e_s >> |U_{ZZ} = \pm 15\,\mathrm{V}|$, then should be used the system shown in Fig. 3.31.

Terminal *A*, the amplifier ground, is connected to amplifier ground. Common-mode voltage e_s is transmitted through the isolation barrier to a common output terminal *B*, which is connected to measurement system ground. In this structure, the common-mode voltage e_s in the strict sense is not a common-mode voltage, because the input amplifier ground has a voltage potential e_s. On the isolation barrier occurs voltage $u_{is} = e_s$.

It follows that the voltage at the amplifier output, one gets

$$e_o = e_{od} + e_{oi} = A_u\left(e_2 - e_1\right) + \frac{e_s}{\text{IMRR}}. \tag{3.90}$$

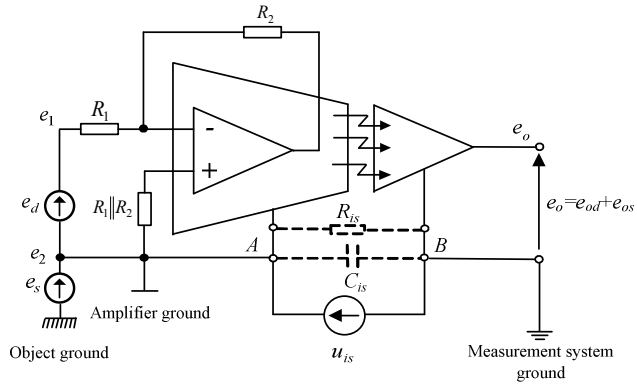


Fig. 3.31. Use of an isolation amplifier when $e_s >> \left|U_{ZZ} = \pm 15\,\text{V}\right|$

When operated isolation amplifiers, the attention should be paid not only for the voltage in the object, but also on the charge stored in this object. Often discussed amplifiers are damaged by flow of the high-value charge, which causes overvoltages in the amplifiers input circuits.

Table 3.4 shows the typical parameters of isolation amplifiers

Isolation amplifiers working properly when:

1. cables leading signals to the amplifier are twisted and shielded.
2. external capacitances will be minimized and balanced in relation to amplifier input and output terminals. This operation minimizes processing errors in terms of amplifier IMRR and CMRR factors.
3. external components and amplifier wires are at such a distance from the amplifier as the distance between the input and output. This procedure protects the amplifier from damage.
4. printed circuit boards (PCBs) are isolation layer covered.

Table 3.4. Parameters of isolation amplifiers

Parameter			Burr - Brown			Analog Devices	
			Capacitance couple		Optoelectronic couple	Transformer couple	
			ISO 130	ISO 164	ISO 100	AD 206	AD 210
Differential input resistance		GΩ	0.53	-	-	0.016	10^3
Common-mode input resistance		GΩ/pF		-	0.1	2/4.5	5/5
Input offset voltage		mV	1	1	05	1	15
Offset voltage drift		$\mu V/^0C$	4.6	5	5	2	2.5
Bias current		nA	670	10^4	1	300	30
Noise voltage		μV_{pp}	250	6	-	2.5	2.0
Noise current		pA_{pp}	-	-	20	-	-
Bandwidth (-3 dB)		kHz	85	0.2	5	100	20
Time response (0.1%)		ms	0.01	0.01	0.1	0.01	0.05
Nonlinearity		%	0.25	0.01	0.4	0.005	0.012
CMRR		dB	72	90	-	100	-
A_u =100		dB	-	-	90	-	120
IMRR A_u =100	DC	dB	140	150	146	-	-
A_u =100	AC (60Hz)	dB	140	115	108	120	-
Max. voltage on isolation barrier		kV	6	1,5	0,75	1,5	2,5
Isolating barrier impedance		GΩ/pF	10^8/0,7	10^8/10	10^6/8	-	-

3.6. SIGNAL SWITCHES

The basic element multiplexers and demultiplexers in the measurement circuit are signals switches. Multiplexers allow to sequential attach multiple signal sources to a single transmission path, however demultiplexers allow to sequential attach many receivers to a transmission path.

Due to the nature of transmitted signals switches are divided into:

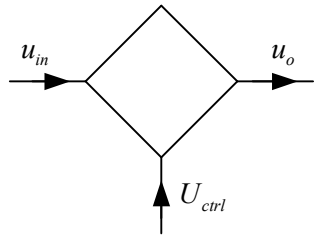
- analog,
- digital.

Analog switches parameters are very important, because they significantly affect the transmitted signals.

We can distinguish switches:

- electromechanical (relays, reed switches, reed switches mercury humidified),
- semiconductor (diode, bipolar, MOS, MOSFET, CMOS, optoelectronic).

Fig. 3.32 presents the analog switch symbol.



$$u_o = u_{in} U_{ctrl}$$

$$U_{ctrl} = \begin{cases} 1 - switch\ conducting \\ 0 - switch\ not\ conducting \end{cases}$$

Fig. 3.32. Switch symbol

Analog switch model is shown in the Fig. 3.33.

In an ideal switch the output voltage is equal to input voltage. In the real switch according to analog switch model scheme, the output voltage depends on many input quantities, including control voltage U_{ctrl} .

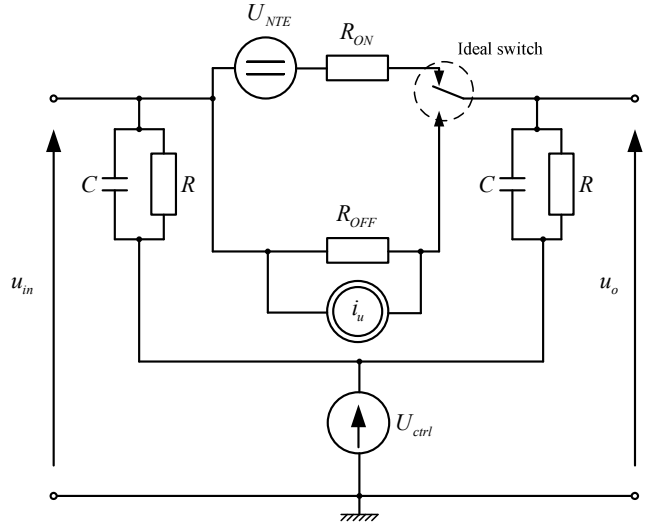


Fig. 3.33. Analog switch model
U_{NTE} – switch thermoelectric voltage,
i_u – switch leakage current,
R_{ON} – switch-on resistance,
R_{OFF} – switch-off resistance,
C, R – capacitance, resistance between control voltage source and switch input and output terminals

Typical switches parameters are presented in Table 3.5.

Switches parameters presented in the Table 3.5 indicates, that contact reed switches has very good electrical parameters, but a disadvantage is a long switching time. The best performance of electronic switches have a FET transistor switch manufactured in CMOS technology.

Table 3.5. Typical analog switches parameters

Parameter	Contact, Reed switch	Diode	Bipolar			FET	
			Normal circuit	Inverse circuit	Compensated inverse circuit	JFET	CMOS
U_{NTE}	μV order	mV order	$(10 \div 500)$mV	1mV	0.1 mV	order of μV	order of μV
i_u	pA order	nA order	1 μA	0.1 μA	0.1 μA	0.5 nA	0.5 nA
$R_{conductive}$	$(0.1 \div 0.01)\Omega$	30 Ω	10 Ω	25 Ω	5 Ω	$(3 \div 300)\Omega$	$(15 \div 800)\Omega$
$R_{notconductive}$	1GΩ	100 MΩ	100 MΩ	100 MΩ	100 MΩ	1GΩ	1GΩ
t_p Switching time	1 ms	0.1 μs	0.1 μs	0.1 μs	0.1 μs	0.2 μs	0.02 μs

4. MATHEMATICAL OPERATIONS REALIZING BY FUNCTIONAL CIRCUITS

4.1. INTRODUCTION

Non-linear mathematical operations, such as: logarithms, exponential function, multiplication, division, exponentiation and square roots, realized by functional circuits, are used to construct nonlinear converters, which allow active, reactive and apparent power measuring, RMS value, resistance, impedance. They are also used in wideband phase shifters and quadrature generators to signals amplitude and phase correction. The principle of multipliers and dividers is done on the basis of systems that operate logarithm and exponential function and time division multiplexing (TDM) systems.

4.2. LOGARITHMIC AND EXPONENTIAL FUNCTIONS CIRCUITS

4.2.1. Principle of operation

The operation of these systems is based on the equations that describe the BJT junction. According to the idealized equation given by Ebers and Moll [3] describing the bipolar transistor *pn* junction, collector current is expressed in relation (Fig. 4.1)

$$i_C = \alpha_F I_{ES}\left(e^{\frac{\frac{u_{BE}}{kT}}{q}} - 1\right) - I_{CS}\left(e^{\frac{-\frac{u_{CB}}{kT}}{q}} - 1\right), \tag{4.1}$$

where: α_F – transistor current gain in the *OB* structure ,
I_{ES}, I_{CS} – junctions saturation reverse currents emitter and collector adequately,
u_{BE}, u_{CB} – *BE i CB* junctions voltages,
q – electric charge 1 eV/V,
k –Baltzmann constant $8{,}62 \cdot 10^{-5}$ eV/K,
T – junction temperature in K.

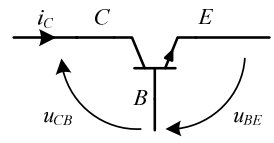


Fig. 4.1. Collector current i_C and the voltages u_{CB} and u_{BE} on transistor *npn* junction

If the transistor work will be realized so that the collector and the base will have the same potential that is $U_{CB} = 0$, then the above equation is transformed into

$$i_C = I_S\left(e^{\frac{\frac{u_{BE}}{kT}}{q}} - 1\right) = I_S\left(e^{\frac{u_{BE}}{U_T}} - 1\right), \tag{4.2}$$

where: I_S – transistor saturation reverse current (it is assumed that for silicon transistor is 0.1 nA, and for germanium 0.1 μA,
U_T – electrokinetic potential, in the junction temperature 300 K, U_T = 26 mV.

Relation $i_C = f(u_{BE})$ was determined experimentally for the two connections of the transistor configuration shown in Fig. 4.2 and shown in the chart (Fig. 4.3) [6].

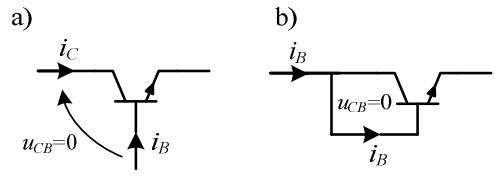


Fig. 4.2. Configurations of transistor connetions, where voltages $u_{CB} = 0$ are obtained by a) uses of system configuration, b) connects collector with base

The voltage at the base emitter junction as shown by Early [6] still depends on the transistor dispersion emitter resistance r_{ee} and base r_{bb} .

$$u_{BE} = \frac{kT}{q} \ln\left(\frac{i_C}{I_S} + 1\right) + i_C r_{ee} + i_B r_{bb} . \tag{4.3}$$

The last word in this formula can be omitted because its value is much lower than the $i_C r_{ee}$ value.

The characteristics of the transdiode junction (Fig. 4.2a) is shown in Fig. 4.3, which from point A to point B with sufficient accuracy for u_{BE} > 100 mV, describes the relation

$$u_{BE} = \frac{kT}{q} \ln \frac{i_C}{I_S} . \tag{4.4}$$

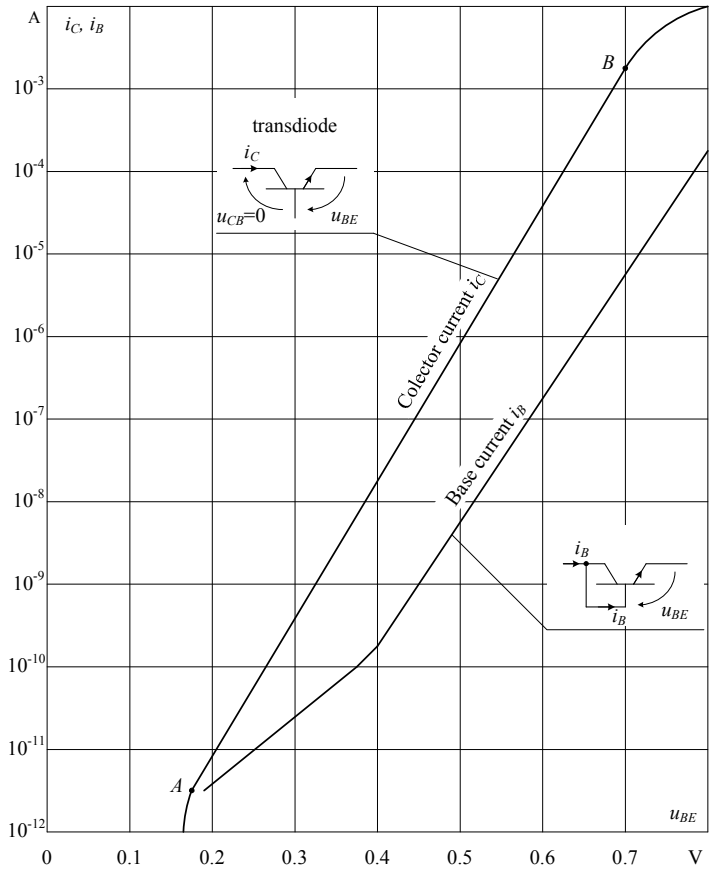


Fig. 4.3. Base – emitter junction characteristics for the transdiode circuit and the collector connected with the base circuit.

Above the point *B* the characteristic is describe by

$$u_{BE} = \frac{kT}{q} \ln \frac{i_C}{I_S} + i_E r_{ee}, \tag{4.5}$$

however below the point *A* is describe by formula

$$u_{BE} = \frac{kT}{q} \ln \left(\frac{i_C}{I_S} + 1 \right). \tag{4.6}$$

These relations indicate that the transistor works in the transdiode connections circuit can be used in the range *AB* for logarithm operations and thus exponential. The logarithm operation, above the point *B* (for currents higher than $1 \cdot 10^{-3}$ A), requires the correction circuit which minimize the effect of the voltage drop on the dispersion emitter resistance on the logarithm operation. Below point A (for

currents less than $1 \cdot 10^{-12}$ A), logarithm operation is carried out with a big error. It follows that, without correction the transistor in transdiode configuration allows logarithms operations in the area of nine decades [25].

Significantly worse properties, as indicated in Fig. 4.3, is obtained by connecting the base with the collector junction. It ensures the logarithm operations realization in the area of six decades. Reduce logarithm operations from the bottom is caused by charge recombination on the base-emitter transistor junction.

Characteristic of silicon transistor *pn* junction is presented in Fig. 4.4.

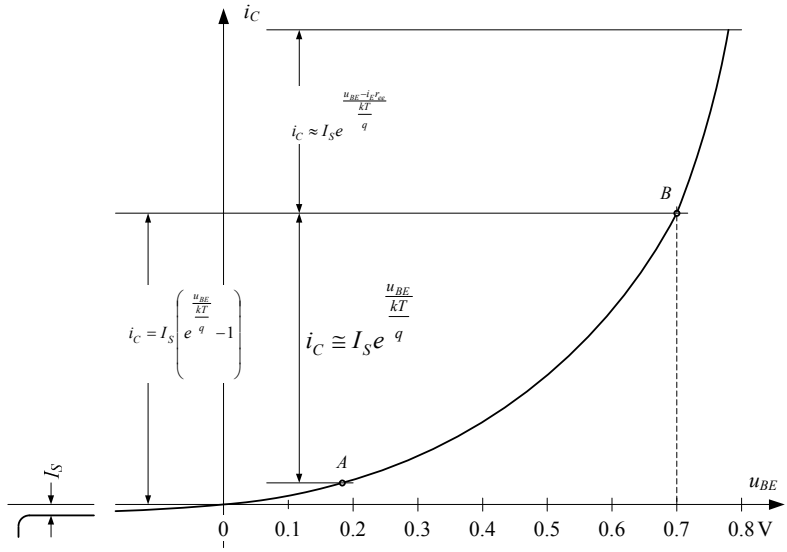


Fig. 4.4. Characteristic of the silicon transistor *pn* junction

Logarithmic and exponential functional circuits is show in Fig. 4.5 [6, 20, 26].

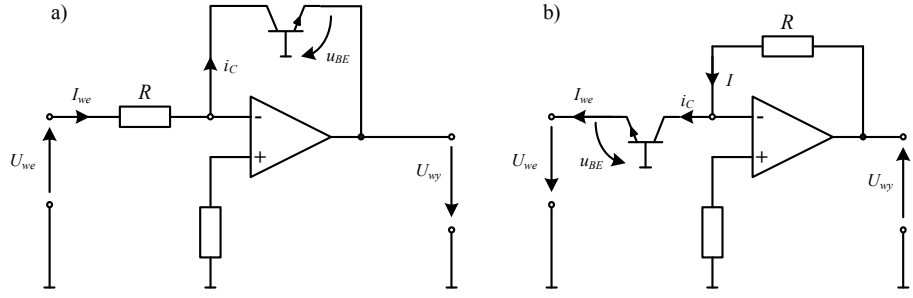


Fig. 4.5. Functional circuits realizing operations
a) logarithmic, b) exponential

Above circuits are adequately described by equations

Logarithm circuit Exponential circuit

$$u_{BE} = U_T \ln \frac{i_C}{I_S}, \qquad i_C = I_S \exp \frac{u_{BE}}{U_T}. \tag{4.7}$$

In this circuits occurs relations

$$I_{in} = i_{C,} \quad u_{BE} = U_{o,} \qquad I = i_C, \quad u_{BE} = U_{in}. \tag{4.8}$$

After substituting this relations to the above equations, one gets

$$U_o = U_T \ln \frac{U_{in}}{RI_S}, \qquad U_o = RI_S \exp \frac{U_{in}}{U_T}, \tag{4.9}$$

Which indicate, that the analyzed circuits realizes logarithm and exponential operations.

Fig. 4.6 shows an effect of dispersion emitter resistance r_{ee} minimizing structure of the transistor on the logarithm operation in the area above the point B (Fig. 4.3 and Fig. 4.4) [6].

If we omit the dispersion base resistance r_{bb} and base current i_B influence then the logarithm circuit output voltage, shown in Fig. 4.6, is

$$U_o = U_T \ln \frac{U_{in}}{RI_S} + i_E r_{ee} - U_{in} \frac{R_2}{R_1 + R_2}. \tag{4.10}$$

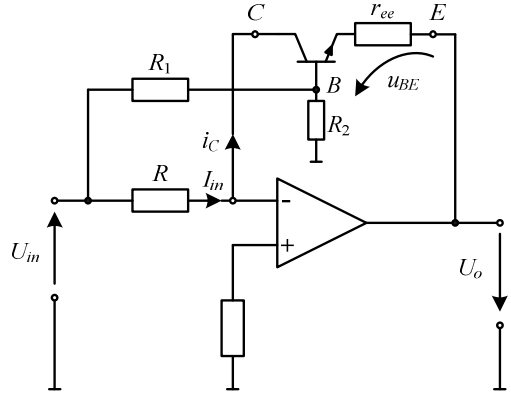


Fig. 4.6. System to minimize the impact of emitter dispersion resistance r_{ee} on the logarithm operation

For large currents values the circuit correctly performs the logarithm operations when

$$i_E r_{ee} - U_{in} \frac{R_2}{R_1 + R_2} = 0 . \tag{4.11}$$

Because $i_E \approx i_C = U_{we}/R$ i $R_1 >> R_2$, so from above relation we get condition to minimize the logarithm error caused by finite value of emitter dispersion resistance r_{ee} .

$$\frac{R_2}{R_1} = \frac{r_{ee}}{R} . \tag{4.12}$$

Example

The top area of logarithmic current is $10 \cdot 10^{-3}$ A. Calculate the resistances of correction resistors R_1 and R_2 if the logarithmic circuit resistance R (Fig. 4.6) is $R = 1 \cdot 10^3\ \Omega$, and emitter dispersion resistance $r_{ee} = 5\ \Omega$.

Assume the resistor value $R_2 = 10\ \Omega$. Then from formula (4.12) is determined

$$R_1 = R \frac{R_2}{r_{ee}} = 1 \cdot 10^3 \frac{10}{5} = 2 \cdot 10^3\ \Omega .$$

Correction resistors values are $R_1 = 2 \cdot 10^3\ \Omega$ i $R_2 = 10\ \Omega$.

4.2.2. Errors caused by elements of circuits

Discussed circuits, in their current form are not applicable to the logarithm or exponential operation, because the U_T and I_S quantities depends on temperature and temperature drift cause significant errors values.

These errors are minimized by using appropriate structure solutions (pairs of the same type transistors), which conduct to compensate effects of temperature drift:

– a good solution when in the transistor pairs the electrokinetic potential drifts U_T and the reverse saturation currents I_S are compensated,

– worse solution when the transistor pairs the reverse saturation currents I_S are compensated and the electrokinetic potential drifts U_T is corrected.

Logarithmic and exponential errors also depend on:

– value of the operational amplifiers input offset voltage V_{os},

– operational amplifiers bias currents I_{BI}, I_{BII},

– symmetry of the transistors parameters,

– emitter dispersion resistance r_{ee} of transistors (for high currents i_C).

4.2.3. Logarithmic circuit realization

Current 10^{-12} A to 10^{-3} A and voltage from 1 mV to 10 V logarithm converter solution is shown in Fig. 4.8 [6, 20]. The processing area lower limit, specify the input offset voltages, input offset voltage drifts, and bias currents of operational

amplifiers. Temperature errors in the converter are corrected with the correct circuit solutions.

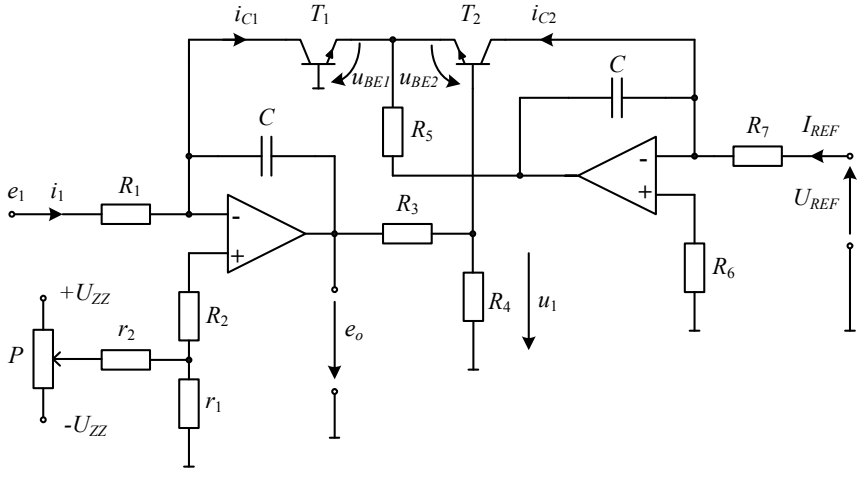


Fig. 4.7. Logarithmic circuit

Monolith transistor pair base voltages are expressed as follows

$$u_{BE1} - u_{BE2} - u_1 = 0\,. \tag{4.13}$$

Having substituted relation (4.4) into above expression, one gets

$$\frac{kT}{q}\ln\frac{i_{C1}}{I_{S1}} - \frac{kT}{q}\ln\frac{i_{C2}}{I_{S2}} = u_1\,. \tag{4.14}$$

This relation, assume that in the monolith transistor pair the reverse saturation currents are both equal $I_{S1} = I_{S2}$, is transformed into

$$u_1 = \frac{kT}{q}\ln\frac{i_{C1}}{i_{C2}}\,. \tag{4.15}$$

If we take into account that the current flowing through the transistor T_2 base is negligibly small compared with the current flowing through the voltage divider formed of resistors R_3, R_4, then

$$e_o = \frac{kT}{q}\frac{R_3 + R_4}{R_4}\ln\frac{i_1}{I_{REF}} = \frac{kT}{q}\frac{R_3 + R_4}{R_4}\ln\frac{e_1}{U_{REF}}\frac{R_7}{R_1}\,. \tag{4.16}$$

As the above equation indicate a converter will be do the logarithm operations properly if the junction temperature T will not affect the processing result.

Minimize the temperature error with a value of +0.33 %/K caused by electrokinetic potential U_T drift is obtained by using:

- R_3 and R_4 resistors with appropriately calculated temperature coefficients, which should be equal to the *pn* junction temperature,
- temperature stabilized *pn* junction circuits.

System processing constant is determined by the values of resistors R_3 and R_4. Resistors R_2 and R_6 minimize the influence of amplifiers bias currents on the circuits operation. In order to reduce processing errors the amplifiers bias currents should be sufficiently small. Resistors r_1, r_2 and potentiometer P allow the system nulling. R_5 and C elements ensure stable converter operation.

4.2.4. Exponential circuit realization

Circuit solution of exponential converter is presented in Fig. 4.8. It is allow to do exponential functions operations on analogical signals values as it was presented in a logarithmic converter [13, 17].

Circuit principle of operations is as follows. Transistors monolithic pair base voltage is described by equation

$$u_1 - u_{BE1} + u_{BE2} = 0\,. \tag{4.17}$$

After entering the relation (4.4) one gets

$$-u_1 = \frac{kT}{q}\ln\frac{i_{C2}}{I_{S2}} - \frac{kT}{q}\ln\frac{i_{C1}}{I_{S1}}\,. \tag{4.18}$$

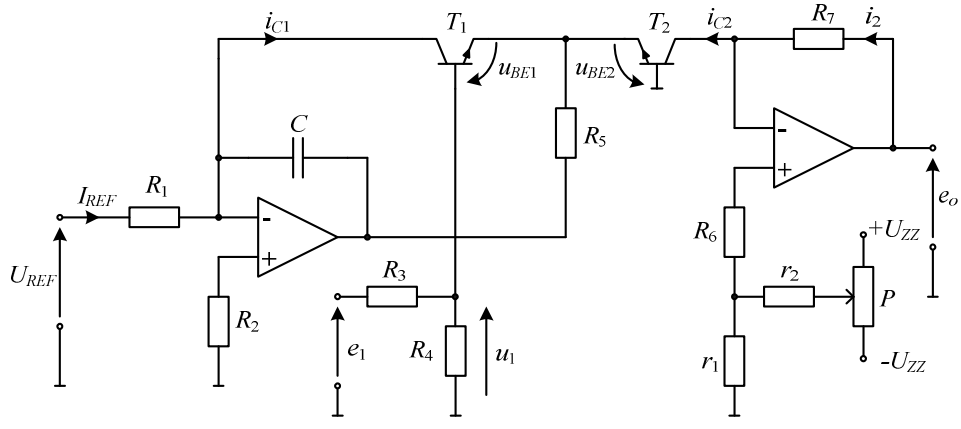


Fig. 4.8. Exponential circuit

Taking into account the relation between voltages u_1 and e_1, were obtained

$$-e_1\frac{R_4}{R_3+R_4} = \frac{kT}{q}\ln\frac{i_{C2}}{i_{C1}}\,. \tag{4.19}$$

Since $i_{C2} = e_o/R_7$, and the current flow through collector of transistor T_1

$$i_{C1} = I_{REF} = \frac{U_{REF}}{R_1}, \tag{4.20}$$

where: U_{REF} – reference voltage,

then relation (4.19) takes the form

$$e_o = R_7 I_{REF} e^{-e_1 \frac{R_4}{R_3+R_4}\frac{q}{k \cdot T}}. \tag{4.21}$$

Converter exponential operation depends on the temperature *pn* junction. Operation error is corrected using the same methods as in the logarithm converter.

The parameters of typical converters realizing the logarithmic and exponential functions of are given in Table 4.1.

Table 4.1. The parameters of converters realizing the logarithmic and exponential functions

System	755N/755P	LOG 100
Processing constant error	±1% ± 0.04%/°C	±0.3% ± 0.03 %/°C
Bias current	10 pA	1 pA
Input offset voltage	0.4mV	1mV
Logarithmic current area	1 nA.....1 mA	1 nA.....1 mA
Exponential voltage area	1 mV.....10 V	1 mV.....10 V
Additional information	755N – realizes negative voltage logarithm operation 755P – realizes positive voltage logarithm operation	realizes logarithm of the current quotient

4.3. MULTIPLIER-DIVIDER CIRCUITS

The multiplier-divider circuit, when the properties of pn junction are used, doing math operations according to principle shown in Fig. 4.9 [13, 17, 27].

Input signals U_x, U_y, i U_u are logarithmic and the voltage at the output of summing point is

$$U_\vartheta = \ln U_x + \ln U_y - \ln U_u = \ln \frac{U_x U_y}{U_u}. \tag{4.22}$$

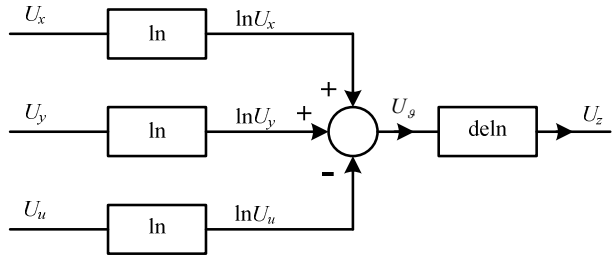


Fig. 4.9. Illustration of multiplier-division principle of operations

Then the voltage is processed in the exponential circuit

$$U_z = e^{U_g} = e^{\ln \frac{U_x U_y}{U_u}} = \frac{U_x U_y}{U_u}. \tag{4.23}$$

According to this principle, the operation of multiplication and division in the circuit shown in Fig. 4.10 is realized. These working refine the operations on the signals U_x, U_y and U_u to the first quarter area of a rectangular coordinates.

The circuit operation is based on a voltages comparison on the base-emitter junctions of transistors T_x, T_y, T_u and T_z. related to formula

$$U_{BEx} + U_{BEy} = U_{BEu} + U_{BEz}. \tag{4.24}$$

Voltages on transistors T_x, T_y, T_u junctions according to relation (4.4) are

$$\begin{aligned} U_{BEx} &= \frac{kT}{q} \ln \frac{U_x}{R_x I_{Sx}}, \\ U_{BEy} &= \frac{kT}{q} \ln \frac{U_y}{R_y I_{Sy}}, \\ U_{BEu} &= \frac{kT}{q} \ln \frac{U_u}{R_u I_{Su}}. \end{aligned} \tag{4.25}$$

By substituting equations (4.25) to the relation (4.24), one gets

$$U_{BEz} = \frac{kT}{q} \ln \frac{U_x U_y}{U_u} \frac{R_u}{R_x R_y} \frac{I_{Su}}{I_{Sx} I_{Sy}}. \tag{4.26}$$

In the analyzed voltage area a collector current I_{Cz} of transistor T_z is related to voltage U_{BEz} by equation

$$I_{Cz} = I_{Sz} \exp\left(\frac{q}{kT} U_{BEz} \right). \tag{4.27}$$

Taking into account, that

$$I_{Cz} = \frac{U_z}{R_z} \tag{4.28}$$

and substituting above relations to equation (4.26), and assuming that *pn* junctions have the same temperature were obtained

$$U_z = \frac{U_x U_y}{U_u} \cdot \frac{R_u R_z}{R_x R_y} \cdot \frac{I_{Su} I_{Sz}}{I_{Sx} I_{Sy}} . \tag{4.29}$$

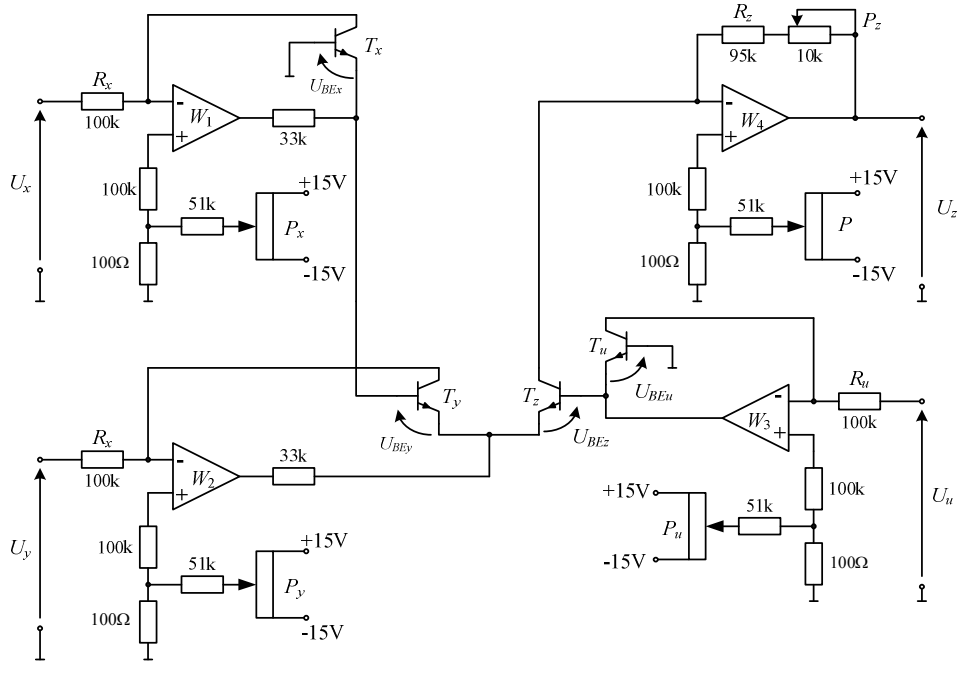


Fig. 4.10. Multiplier – divider circuit

In the multiplier – divider circuits uses monolithic transistors have the same properties because they are made in a single semiconductor crystal, in one technological process, and therefore a reverse saturation currents are equal

$$I_{Sx} = I_{Sy} = I_{Su} = I_{Sz} . \tag{4.30}$$

Hence, the relation (4.29) is

$$U_z = c \frac{U_x U_y}{U_u} , \tag{4.31}$$

where: $c = \dfrac{R_u R_z}{R_x R_y}$ - multiplier – divider circuit processing constant.

The presented analysis shows that the multiplication and division operations accuracy depends on:

- Transistors parameters identity,
- Operational amplifiers properties,
- Accuracy and value stability of resistors R_x, R_y, R_u and R_z.

Multiplier - divider AD 434 manufactured by Analog Devices has the following parameters [34]

- Processing error constant $\pm 0{,}2\,\% \pm 0{,}01\,\%/^{\circ}\mathrm{C}$,
- Output offset voltage $V_{oso} = \pm 1\mathrm{mV}$,
- Input voltage range $0{,}1 < U_x, U_y, U_u \leq 10\ \mathrm{V}$,
- Bandwidth (-3 dB) 100 kHz,
- Slew rate $\mathrm{SR} = 2\ \mathrm{V}/\mu\mathrm{s}$.

4.4. MULTIFUNCTIONAL ANALOG TRANSDUCER

Converter math operations are conducted on the principle of logarithm and exponential function basis. The following direct operation are realized by this converter: multiplication, division, square roots and exponents of one quantity or two quantities ratio. However, indirectly, when the output signal is transmitted to one of the inputs, the converter allows to perform complex mathematical operations.

The multifunctional operating converter structural circuit is illustrated in Fig. 4.11. [13, 17, 18, 27,]

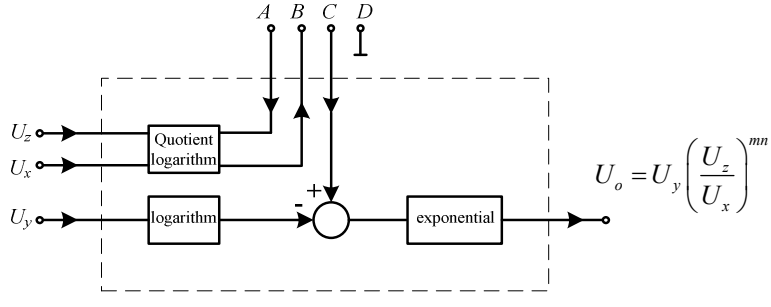


Fig. 4.11. Structural circuit of multifunctional converter

Output voltage

$$U_o = U_y \left(\frac{U_z}{U_x} \right)^{mn}, \tag{4.32}$$

where: U_x, U_y, U_z – input voltages,

m, n – exponents given by external resistors values attached to points A, B, C and D.

U_x, U_y, U_z voltages can take positive values in the range from 0.1 V to 10 V, while the product of mn can be selected in the range from 0.2 to 5.

Combining the multiplication, division, exponentiation and root functions within a single converter provides it computing power comparable to the computational power of small analog machine.

A typical solution of multifunctional converter shown in Fig. 4.12 contains four operational amplifiers, two symmetrical pairs of monolithic transistors and eight high resistance stability resistors, wherein four resistors R_1, R_2, R_3 and R_4 form an external bridge circuit.

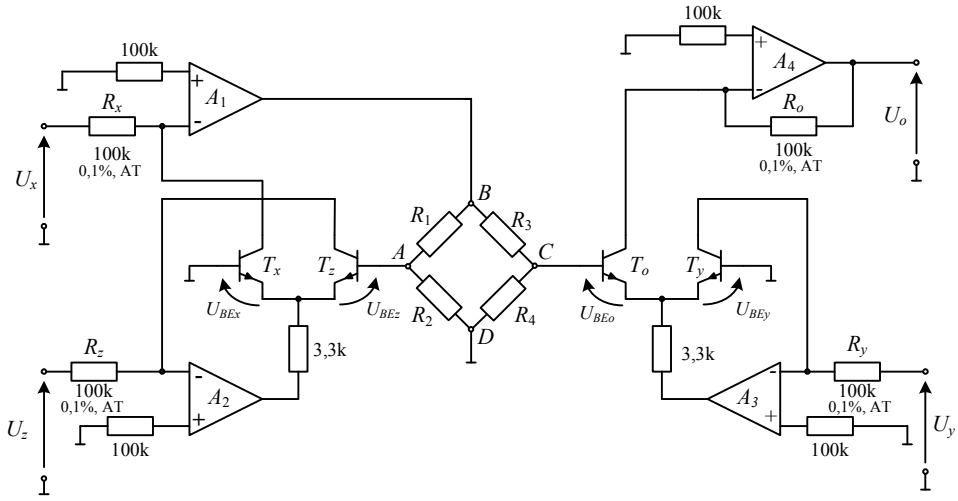


Fig. 4.12. Structural solution of a multifunctional converter

In this structure uses the relations between U_{BD} voltage and U_{AD} and U_{CD} voltages, which are equal to voltages on the base-emitter junctions, respectively, on transistors T_x, T_z and T_y, T_o.

According to Fig. 4.12 the U_{AD} voltage is

$$U_{AD} = U_{BEz} - U_{BEx}, \tag{4.33}$$

which, after considering the formula (4.4) takes the form

$$U_{AD} = \frac{kT}{q} \ln \frac{I_z I_{Sx}}{I_x I_{Sz}} = \frac{kT}{q} \ln \frac{U_z R_x}{U_x R_z}. \tag{4.34}$$

Similarly we got

$$U_{CD} = U_{BEo} - U_{BEy} = \frac{kT}{q} \ln \frac{U_o R_y}{U_y R_o}. \tag{4.35}$$

Voltages U_{AD} and U_{CD}, as defined by (4.34) and (4.35), are also equal to voltage drops respectively occurring on the resistors R_2 and R_4, caused by the output voltage U_{BD} of operational amplifier A_1. Operational amplifier A_1 output voltage U_{BD} is a function of voltages U_x and U_z. Bridge circuit voltages U_{AD} and U_{CD} associated with the voltage U_{BD} following relations

$$\begin{aligned} U_{AD} &= U_{BD} \frac{R_2}{R_1 + R_2}, \\ U_{CD} &= U_{BD} \frac{R_4}{R_3 + R_4}, \end{aligned} \tag{4.36}$$

assuming that the bridge currents are incomparably higher than the transistors T_z and T_o base currents.

In the practical solutions it is assumed, that equations (4.36) are realized with enough accuracy, when $50\Omega < R_{1,\ldots,}R_4 < 300\Omega$. After solving the system of equations (4.34) – (4.36), one gets

$$\ln\left(\frac{U_o}{U_y}\frac{R_y}{R_o}\right) = \ln\left(\frac{U_z}{U_x}\frac{R_x}{R_z}\right)^{\frac{R_4}{R_3+R_4}\frac{R_1+R_2}{R_2}}, \tag{4.37}$$

And after exponential, one gets

$$U_o = \frac{R_o}{R_y} U_y \left(\frac{R_x}{R_z}\frac{U_z}{U_x}\right)^{mn}, \tag{4.38}$$

where:

$$m = \frac{R_4}{R_3 + R_4} \le 1, \qquad n = \frac{R_1 + R_2}{R_2} \ge 1.$$

If the condition of equal resistance will be done

$$R_o = R_y \quad \text{and} \quad R_x = R_z,$$

then

$$U_o = U_y \left(\frac{U_z}{U_x} \right)^{mn} . \tag{4.39}$$

This operation accuracy depends on the symmetry of the bipolar transistors pairs, operational amplifiers characteristics and resistors parameters.

Multifunctional operating converter AD 538 (Analog Devices) parameters are as follows:

- Processing constant error $\pm 0.25\% \pm 0.01\%/°C$,
- Output offset voltage $V_{oso} = \pm\ 0.25$ mV,
- Input voltages range $0.1\text{V} \leq U_x, U_y, U_z \leq 10$ V,
- Bandwidth (-3 dB) 400 kHz,
- Slew rate $SR = 1.4\,\text{V}/\mu\text{s}$.

Analyzed computing capabilities of illustrated converter are presented in Table 4.2.

Table 4.2. Fundamental errors of selected operation realized by Burr Brown multifunctional converter

Mathematical operations	Operation errors
Multiplication	± 0.25 %
Division	± 0.25 %
Square	±0.3 %
Square root	± 0.7 %
Exponentiation, 5th order index	± 1.5 %
Root, 5th order index	±2 %
sinΘ	±0.5 %
cosΘ	±0.8 %
Argument $\varphi = arctg(U_y / U_x)$	±0.6 %
Module $\sqrt{U_x^2 + U_y^2}$	±0.7 %

In the Table 4.2 detailed basic math errors. In the converter total errors determination should be respected the operating converter output offset voltage caused by converter temperature drift and the external components errors. For example, when the circuit performs:

- exponentiation, it is necessary to determine the effect of resistors R_1 and R_2 on the processing error,
- square it is necessary to determine the effect of resistors R_3, R_4 on the processing error.

4.5. MULTIPLIERS WITH CONTROLLED CURRENTS DIVISION

4.5.1. Multipliers with controlled currents division - principle of operation

Multipliers with controlled currents division, are a modification of variable multipliers with variable transconductance, allowing you to carry out multiplication and division operations in the four quadrants, for voltages in the range of ±10V. Multiplication and division operations accuracy in the best circuits is realized with an error no greater than 0.1%. The advantages of this multipliers class include: wide bandwidth, differential input, small errors, good linearity and low price. It dominated the market and are offered in different variants. Applied technology and system solutions, including laser jet correction systems have led to a multiplier, which in standard applications do not require any additional components.

Multiplier with controlled currents division is show in Fig. 4.13. Signal multiplication and division operation is realized on the three transistors pairs, through which currents of controlled current sources, divided with using a voltage followers [17].

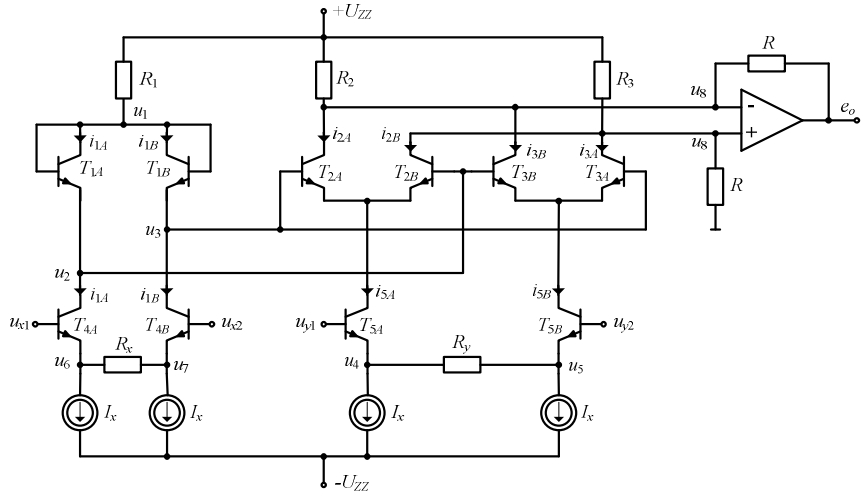


Fig. 4.13. Multiplier with controlled currents division

Voltages on the transistors T_{1A} and T_{1B} *BE* junctions depend on the relation (4.4) and are described by equations

$$\begin{aligned} u_1 - u_2 &= \frac{kT_{1A}}{q} \ln \frac{i_{1A}}{I_{S1A}}, \\ u_1 - u_3 &= \frac{kT_{1B}}{q} \ln \frac{i_{1B}}{I_{S1B}}. \end{aligned} \tag{4.40}$$

Assuming, that the transistors at the analyzed circuit are made from one crystal and in one technological process, and they have the same temperature, then from equations (4.40), one gets

$$u_3 - u_2 = \frac{kT}{q} \ln \frac{i_{1A}}{i_{1B}}. \tag{4.41}$$

Similar relations got for transistors pairs T_{2A} and T_{2B}, T_{3A} and T_{3B}

$$u_3 - u_2 = \frac{kT}{q} \ln \frac{i_{2A}}{i_{2B}}, \tag{4.42}$$

$$u_3 - u_2 = \frac{kT}{q} \ln \frac{i_{3A}}{i_{3B}}. \tag{4.43}$$

From equations (4.41), (4.42) and (4.43) follows that

$$\frac{i_{1A}}{i_{1B}} = \frac{i_{2A}}{i_{2B}} = \frac{i_{3A}}{i_{3B}}. \tag{4.44}$$

Assumed that the operational amplifier is ideal and the amplifier input voltage $u_8$is equal to the non-inverting input voltage.

The sum of currents at the inverting input

$$\frac{U_{ZZ} - u_8}{R_2} = i_{2A} + i_{3B} + \frac{u_8 - e_o}{R}. \tag{4.45}$$

Similar relation we have for non-inverting input

$$\frac{U_{ZZ} - u_8}{R_2} = i_{2B} + i_{3A} + \frac{u_8}{R}. \tag{4.46}$$

From equations (4.45) and (4.46) we gets

$$\frac{e_o}{R} = i_{2A} - i_{2B} - i_{3A} + i_{3B}. \tag{4.47}$$

Similarly, we describe the voltage on junctions of transistors pair T_{4A} and T_{4B}, and we obtain

$$u_{x1} - u_6 = \frac{kT}{q} \ln \frac{i_{1A}}{I_{S4A}}, \tag{4.48}$$

$$u_{x2} - u_7 = \frac{kT}{q} \ln \frac{i_{1B}}{I_{S4B}}. \tag{4.49}$$

Subtracting these equations we get

$$u_{x1} - u_{x2} = u_6 - u_7 + \frac{kT}{q} \ln \frac{i_{1A}}{i_{1B}} . \tag{4.50}$$

These currents of transistors flow through emitters and are equal

$$i_{1A} = \frac{u_6 - u_7}{R_x} + I_x , \tag{4.51}$$

$$i_{1B} + \frac{u_6 - u_7}{R_x} = I_x . \tag{4.52}$$

From equations (4.51) and (4.52) we get

$$i_{1A} + i_{1B} = 2I_x . \tag{4.53}$$

Substituting $u_6 - u_7$ from equation (30.12) to formula (30.11) we get

$$u_{x1} - u_{x2} = (i_{1A} - I_x)R_x + \frac{kT}{q} \ln \frac{i_{1A}}{i_{1B}} . \tag{4.54}$$

Having substituted above relation into expression (4.55) we eliminate I_x quantity

$$u_{x1} - u_{x2} = \frac{R_x}{2}(i_{1A} - i_{1B}) + \frac{kT}{q} \ln \frac{i_{1A}}{i_{1B}} . \tag{4.55}$$

To simplify the discussion a logarithm in equation (4.55) can be omitted. This procedure introduces relatively small error of a non-linear character. Then the equation (4.55) is written

$$u_{x1} - u_{x2} = \frac{R_x}{2}(i_{1A} - i_{1B}) . \tag{4.56}$$

Similar discussion is done for transistors pair T_{5A} and T_{5B} and we get

$$u_{y1} - u_{y2} = \frac{R_y}{2}(i_{5A} - i_{5B}) . \tag{4.57}$$

From equations (4.56) and (4.57) we obtain

$$\frac{4(u_{x1} - u_{x2})(u_{y1} - u_{y2})}{R_x R_y} = (i_{1A} - i_{1B})(i_{5A} - i_{5B}) . \tag{4.58}$$

Currents flowing through transistors collector T_{5A} and T_{5B} are equal

$$\begin{aligned} i_{5A} &= i_{2A} + i_{2B} , \\ i_{5B} &= i_{3A} + i_{3B} . \end{aligned} \tag{4.59}$$

On the basis of equations (4.53) and (4.44) the currents i_{1A} and i_{1B} was expressed with currents i_{2A}, i_{2B} and I_x

$$\begin{aligned} i_{1A} &= 2I_x \frac{i_{2A}}{i_{2A}+i_{2B}}, \\ i_{1B} &= 2I_x \frac{i_{2B}}{i_{2A}+i_{2B}}. \end{aligned} \tag{4.60}$$

By introducing the equations (4.59) and (4.60) to relation (4.58), one gets

$$\frac{4(u_{x1}-u_{x2})(u_{y1}-u_{y2})}{R_x R_y} = 2I_x \left[i_{2A} - i_{2B} - (i_{3A}+i_{3B}) \frac{i_{2A}-i_{2B}}{i_{2A}+i_{2B}} \right]. \tag{4.61}$$

From relation (4.44) follows, that

$$\frac{i_{2A}-i_{2B}}{i_{2A}+i_{2B}} = \frac{i_{3A}-i_{3B}}{i_{3A}+i_{3B}}. \tag{4.62}$$

Taking into consideration this formula in the equation (4.61) we have

$$\frac{4(u_{x1}-u_{x2})(u_{y1}-u_{y2})}{R_x R_y} = 2I_x (i_{2A}-i_{2B}-i_{3A}+i_{3B}). \tag{4.63}$$

From relations (4.63) and (4.47) comparison finally obtained

$$e_o = \frac{2R}{R_x R_y} \frac{(u_{x1}-u_{x2})(u_{y1}-u_{y2})}{I_x}. \tag{4.64}$$

This equation indicates that the analyzed circuit performs multiplication operations on the differential signals $u_{x1} - u_{x2}$, $u_{y1} - u_{y2}$ and division by current I_x. There are two multipliers circuit solutions. If the current I_x is a constant value, then the current is provide to a multiplier constant. If the current I_x is controlled then this circuit is a multiplier-divider circuit. The best multipliers, operating under the discussed principle, possible operations of multiplication and division with an error of 0.1%.

This error value have modified multipliers shown in Fig. 4.14. The signal amplifier is an instrumentation amplifier with source currents (I) and two additional inputs Z_1 (Reference), Z_2 (Sense). This solution eliminates the non-linearity error of logarithm operations defined by the relation (4.55).

The circuit solution shown in Fig. 4.14 has several advantages [17]:

- multiplier has low sensitivity to voltage drift,
- the circuit realizing division operation have a feedback,
- differential inputs of multiplier-divider circuit with high input impedance,
- better slew rate parameter because the feedback makes the pole is eliminated by zero of multiplier-divider circuit.

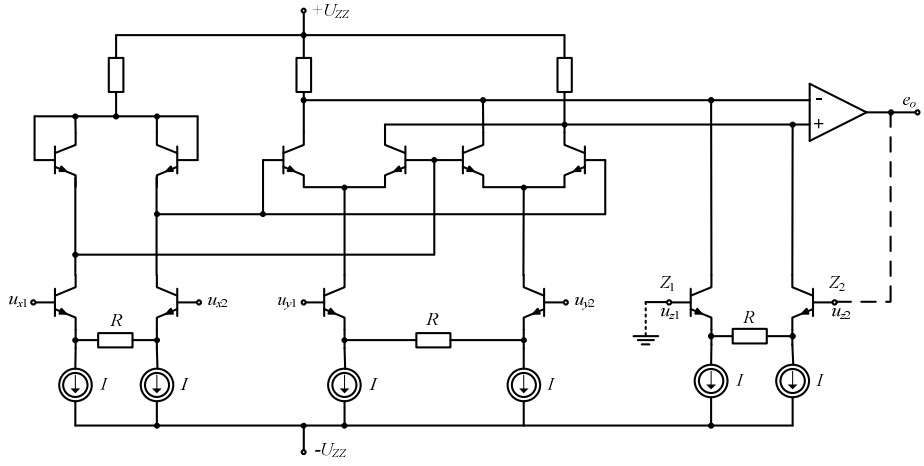


Fig. 4.14. Modified multiplier-divider circuit

This class of represent components whose parameters are given in Table 4.3.

Table 4.3. Parameters of multiplier-dividers and multipliers with controlled currents division

Circuit	AD734	AD 633	AD 632 MPY 100	AD 534 MPY 534	MPY 634
Operation	$\frac{xy}{U}+z$	$\frac{xy}{10}+z$	$\frac{xy}{E_R}+z$	$\frac{xy}{E_R}+z$	$\frac{xy}{E_R}+z$
Processing constant error	±0.1% ±0.004%/°C	±1% ±0.01%/°C	±0.5% ±0.01%/°C	±0.5% ±0.005%/°C	±0.5% ±0.01%/°C
Input offset voltage X_{os}, Y_{os} Z_{os}	 5 mV 5 mV	 5 mV 1 mV	 2 mV 2 mV	 2 mV 2 mV	 5 mV 5 mV
Bandwidth (-3dB), for low signals < 0,1V	100 MHz	1 MHz	1 MHz	1 MHz	10 MHz
Bandwidth with error 1%	1 MHz	50 kHz	50 kHz	70 kHz	100 kHz
Slew rate	400 V/μs	20 V/μs	20 V/μs	20 V/μs	20 V/μs
Operation errors division exponential root	 ±0.1% ±0.1% -	 - ±1% -	 ±0.35% ±0.3% ±0.5%	 ±0.35% ±0.3% ±0.5%	 ±0.35% ±0.3% ±0.5%
Additional information	precise	cheap	The same configured terminals	The same configured terminals	Terminals as in MPY 534

4.5.2. Use of multipliers with controlled currents division

In the section (4.5.1) discussed two classes of multipliers with controlled currents division. The multiplier shown in Fig. 4.13 has the output amplifier with a constant, specific gain value. The multiplier shown in Fig. 4.14 has the output amplifier with an unspecified gain value, tending to infinity. The principle of operation the first multiplier (Fig. 4.13) is typical, while use of the second multiplier (Fig. 4.14) requires clarification.

Structural scheme of multiplier with the output amplifier with gain tending to infinity is show in Fig. 4.15 [23, 27].

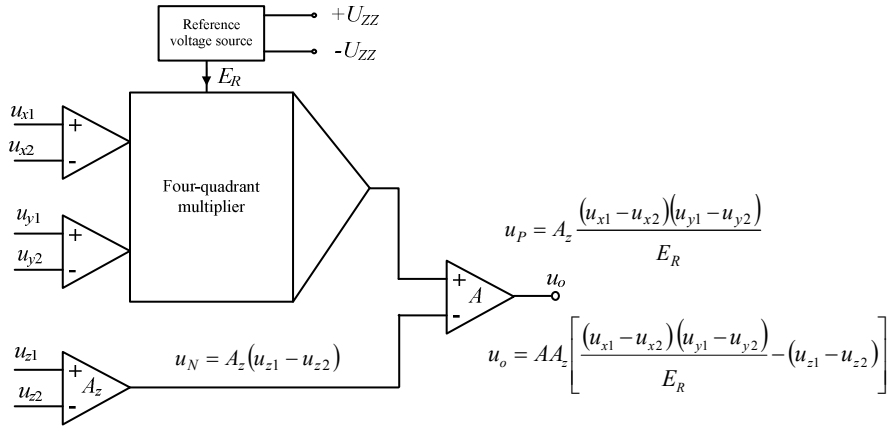


Fig. 4.15. Structural scheme of a multiplier with the output amplifier with infinite gain

The output voltage of four-quadrant multiplier is described by formula

$$u_P = A_z \frac{(u_{x1} - u_{x2})(u_{y1} - u_{y2})}{E_R}, \tag{4.65}$$

where: A_Z – the processing constant,

E_R – a reference voltage set by multiplier user, usually this value is equal 10.

Output voltage of differential amplifier, which is connected to inverting input of amplifier with gain A, is equal

$$u_N = A_z(u_{z1} - u_{z2}), \tag{4.66}$$

where: A_z – amplifier gain given during manufacture process.

Because multiplier constant (A_z) and amplifier gain (A_Z) have the same value, then the multiplier output voltage u_o is

$$u_o = A(u_P - u_N) = AA_z\left[\frac{(u_{x1}-u_{x2})(u_{y1}-u_{y2})}{E_R} - (u_{z1}-u_{z2})\right]. \qquad (4.67)$$

The gain A of output amplifier is very high, thus can be assume that $AA_z \to \infty$ and the above formula can be written as

$$(u_{x1}-u_{x2})(u_{y1}-u_{y2}) = E_R(u_{z1}-u_{z2}), \qquad (4.68)$$

which will form the basis for multipliers, dividers and converters configure.

The block scheme of analyzed multiplier is presented in Fig. 4.16.

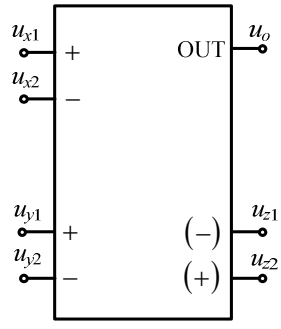


Fig. 4.16. Simplified block scheme of a multiplier shown in Fig. 4.15

The system shown in Fig. 4.15 shows that the output of an amplifier with the gain A_Z is connected to the inverting input amplifier with the gain A. This causes that for multiplier the input u_{Z1} is an inverting input, and the input u_{Z2} is a non-inverting input. In the multiplier will be realized negative feedback loop if the output signal u_o will be transmitted to the one of inverting inputs u_{x2}, u_{y2}, or u_{Z1}.

Here are some examples of functional circuits.

Multiplier with differential inputs

We use the main equation (4.68)

$$(u_{x1}-u_{x2})(u_{y1}-u_{y2}) = E_R(u_{z1}-u_{z2}).$$

If, in accordance with above principles, we will assume that

$$u_{z1} = u_o, \qquad \text{a} \qquad u_{z2} = 0,$$

then

$$(u_{x1}-u_{x2})(u_{y1}-u_{y2}) = E_R u_o,$$

hence

$$u_o = \frac{(u_{x1}-u_{x2})(u_{y1}-u_{y2})}{E_R}.$$

This equation is realized by circuit presented in Fig. 4.17.

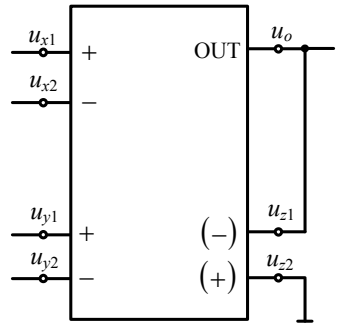


Fig. 4.17. Multiplier with differential inputs

Differential signals divider

If into general relation

$$(u_{x1} - u_{x2})(u_{y1} - u_{y2}) = E_R(u_{z1} - u_{z2}),$$

we are substituting equations

$u_{y1} = 0$, and $u_{y2} = u_o$,

then we get

$$u_o = -E_R \frac{u_{z1} - u_{z2}}{u_{x1} - u_{x2}}.$$

This equation is realized by circuit presented in Fig. 4.18.

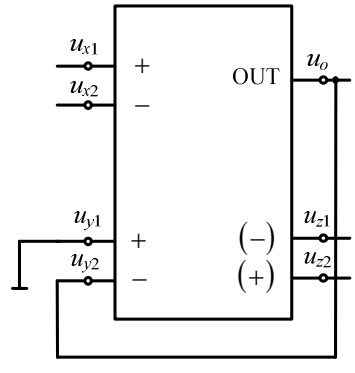


Fig. 4.18. Differential signals divider

Square rooter

If to the main relation we are substituting

$u_{x1} = u_{y1} = u_{z2} = 0$, $u_{x2} = u_{y2} = u_o$ and $u_{z1} = u_A$,

Then we get

$$(0 - u_o)(0 - u_o) = E_R u_A,$$

And after transformation

$$u_o = \sqrt{E_R u_A}\ .$$

Diode connected to the circuit output prevents rooter saturation. (Fig. 4.19). In this circuit, negative feedback will also be executed when the output voltage u_o is given to the inverting inputs u_{x1} and u_{y1}.

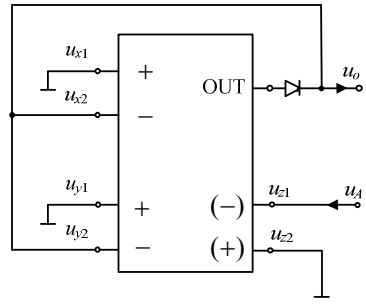


Fig. 4.19 Square rooter

Circuit realizing difference of power to two

If to the main relation we are substituting relations

$$u_{x1} = u_A,\ u_{x2} = u_{y1} = \frac{u_A + u_B}{2},\quad u_{z1} = \frac{u_0}{4}\quad i\quad u_{y2} = u_{z2} = 0,$$

then we get

$$\left(u_A - \frac{u_A + u_B}{2}\right)\left(\frac{u_A + u_B}{2} - 0\right) = E_R \frac{u_o}{4}\ .$$

Finally

$$u_o = \frac{u_A^2 - u_B^2}{E_R}\ .$$

This equation is realized by circuit presented in Fig. 4.20.

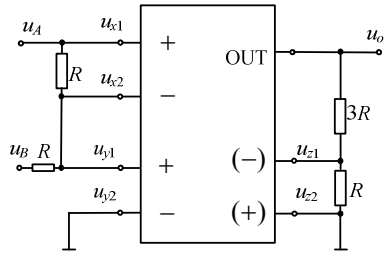


Fig. 4.20. Circuit realizing the difference of power to two

RMS converter

Idea of RMS converter built on the multiplier is presented in the Fig. 4.21.

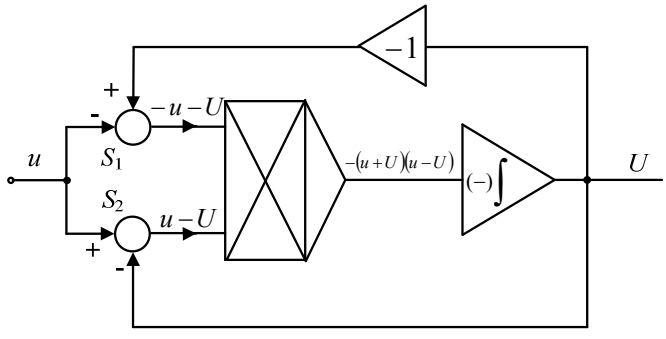


Fig. 4.21. Structural scheme illustrating an idea of RMS principle of operation

Input voltage u is summed up in nodes S_1 and S_2 with the converter output voltage U. Then the sum and difference of these voltages is fed to the inputs of multiplier. In steady state the output voltage of multiplier

$$u_o = -(u+U)(u-U),$$

is averaged in the integrator with a processing constant k_c according to the formula

$$U = -k_c \frac{1}{T}\int_0^T u_o dt = k_c \frac{1}{T}\int_0^T (u+U)(u-U)\,dt\,.$$

The above relation is written as

$$\frac{U}{k_c} = \frac{1}{T}\int_0^T \left(u^2 - U^2\right)dt\,.$$

If the integrating constant k_c is enough large, then left side of the equation tends to zero and obtained

$$\frac{1}{T}\int_0^T u^2 dt = \frac{1}{T}\int_0^T U^2 dt = U^2 .$$

It follows that the converter output voltage is characterized by RMS value

$$U = \sqrt{\frac{1}{T}\int_0^T u^2 dt} .$$

In the analyzed converter the square root circuit does not exist. It was obtained by using a multiplier with two negative feedback loops. This idea of RMS converter working is realized by multiplier-divider circuit shown in Fig. 4.22, which describe a similar equation. The output u_o connection with the input u_{z1} indicates that multiplier-divider is configured as a multiplier (Fig. 4.17) and its output voltage is

$$u_o = -\frac{(u+U)(u-U)}{E_R} .$$

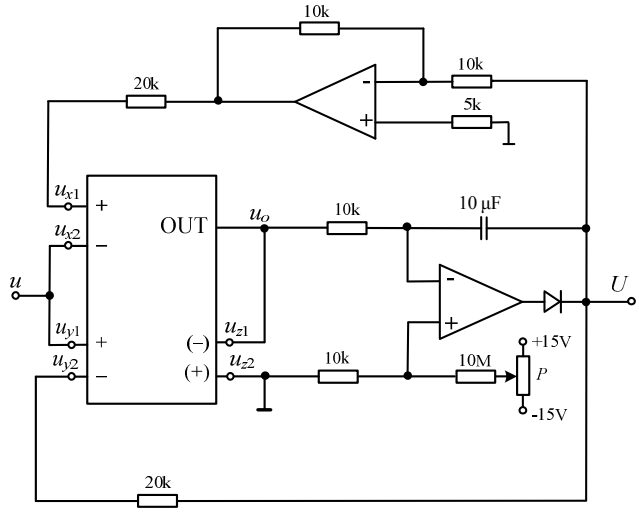


Fig. 4.22. RMS converter built on the multiplier-divider circuit

Using the above relations these voltage after integration can be presented as

$$\frac{1}{T}\int_0^T \frac{u^2 - U^2}{E_R} dt = 0 .$$

Finally, the RMS converter output voltage

$$U = \sqrt{\frac{1}{T}\int_0^T u^2 dt} .$$

The analyzed converter is described by implicit function and has the metrological parameters which characterizing this class of RMS converters.

These examples show that multiplier-dividers with controlled currents division, taking into account create a wide class of converters.

4.6. TIME DIVISION MULTIPLIERS

Time division multipliers, also called TDM multipliers, are the most accurate multipliers. The disadvantage of this multipliers class is limited frequency band of multiplied signals arising from the proper modulation condition, which occurs when the $f_g T << 1$, where f_g - the cut-off frequency of multiplied signals and T - the period of modulate course. In addition, a critical factor for the correct working of multiplier is a modulator switching time. These time should be negligible small compared with the period T. These limitations mean that these systems are used for the multiplication of extremely low frequency signals or low slew rate signals $\left(f_g < 1\text{kHz},\ SR < 0.7\,\text{V/ms}\right)$.

Time division multipliers perform multiplication operations in the best multipliers with an error of 0.01%. Due to the structure TDM can be divided into circuits with open and close structure. These are complex circuits, not produced in the integrating form and hence are expensive.

The basic TDM circuit with open structure is presented in Fig. 4.23.

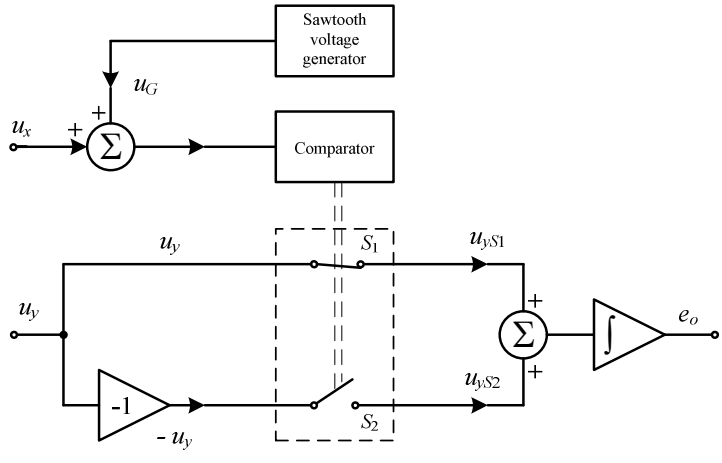


Fig. 4.23. Structural scheme of the basic TDM circuit

Principle of operation of the multiplier is as follows. Processed voltage u_x is given to the summing node, where is also transmitted signal u_G from sawtooth voltage generator. At the adder output is a sawtooth voltage shifted along the ordinate axis by the value of u_x. Then, the voltage is fed to the comparator. At the comparator output is obtained a square wave pulse width t_1 and t_2 (Fig. 4.24). By this course are controlled the switches S_1 and S_2. At the switch S_1 is given voltage u_y, and to the switch S_2 is transmitted voltage u_y. At the switch outputs we have voltages u_{yS1} at the switch S_1 occuring at the time t_2 and at the switch S2 we have voltages u_{yS2} occuring at the time t_1. At the output of an integrating circuit we obtain averaged voltage

$$e_o = \frac{u_y t_2 - u_y t_1}{T}. \tag{4.69}$$

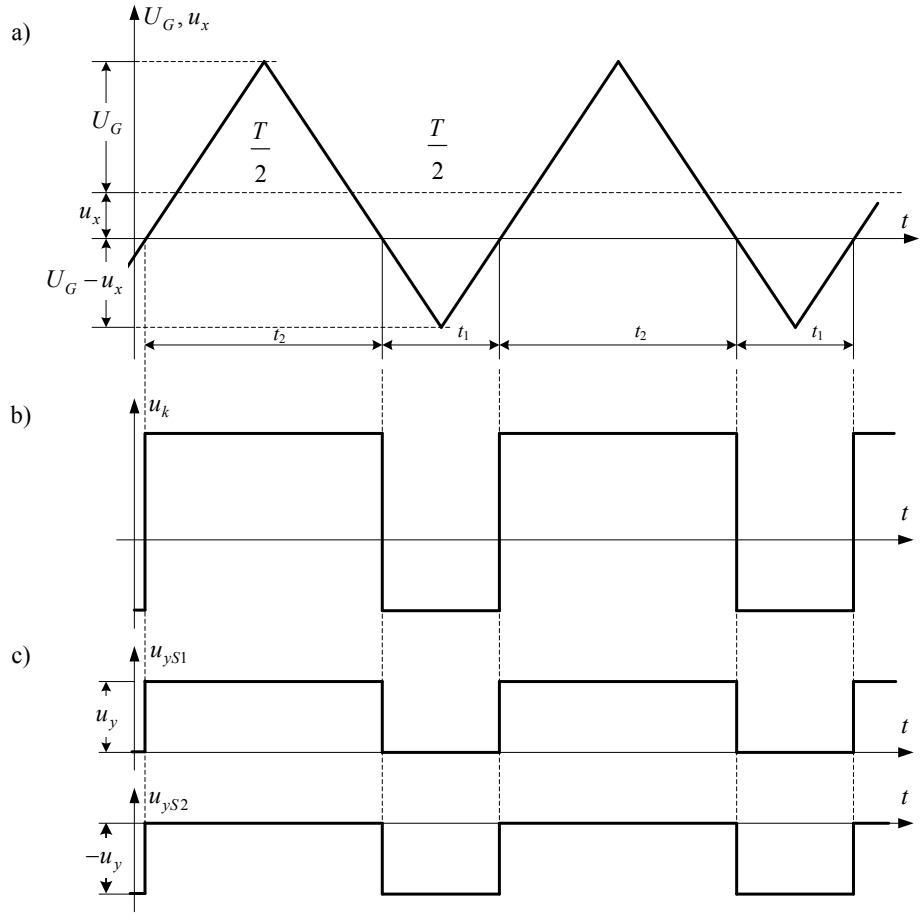


Fig. 4.24. Voltages waveforms in the TDM multiplier
a) – adder node, b) – comparator, c) – switch *S*1, d) – switch *S*2

Relations between time intervals t_1, t_2, a period T, voltages u_x and amplitude U_G determined on the basis of Fig. 4.24a. Here there are relations

$$\frac{\frac{T}{2}}{U_G} = \frac{t_2}{U_G + u_x} \qquad \text{hence} \qquad t_2 = \frac{T}{2}\frac{U_G + u_x}{U_G}, \tag{4.70}$$

$$\frac{\frac{T}{2}}{U_G} = \frac{t_1}{U_G - u_x}, \qquad \text{hence} \qquad t_1 = \frac{T}{2}\frac{U_G - u_x}{U_G}. \tag{4.71}$$

After substituting relations describing t_1 and t_2 to formula (4.69) was obtained

$$e_o = \frac{u_x u_y}{U_G}. \tag{4.72}$$

Multiplication result depends on the voltages u_x and u_y value and the voltage generator amplitude of voltage generator U_G, but does not depend on the signal frequency.

Analyzed multiplier has an open structure, the circuit solution is given in [13], the error of multiplication DC voltages is 0.5%.

Much better parameters has a multiplier with closed structure, which structural scheme is shown in Fig. 4.25 [15]. A TDM multiplier designed by Yokogawa Electric Works carries out the multiplication operation in the band of 2 kHz with an error not exceeding 0.02%.

The analysis was done when the voltages u_x and u_y are DC voltages, and the multiplier voltages reached a steady state. The generator on the output has a sawtooth course voltage e_2, which is compared with the voltage e_1 received from the integrator created from the amplifier A. At the time interval t_2 the voltage $e_1 < e_2$, switches S_1 and S_2 are switching on voltages $+E_s$ and $+u_y$, and capacitor C is charged by sum of currents i_x and i_s. At these capacitor is voltage change given by the formula

$$\Delta u_c = -\frac{1}{C}\int_o^{t_2}(i_x + i_s)dt = -\frac{1}{C}\int_o^{t_2}\left(\frac{u_x}{R_1} + \frac{E_s}{R_2}\right)dt = -\left(\frac{u_x}{R_1} + \frac{E_s}{R_2}\right)\frac{t_2}{C}. \tag{4.73}$$

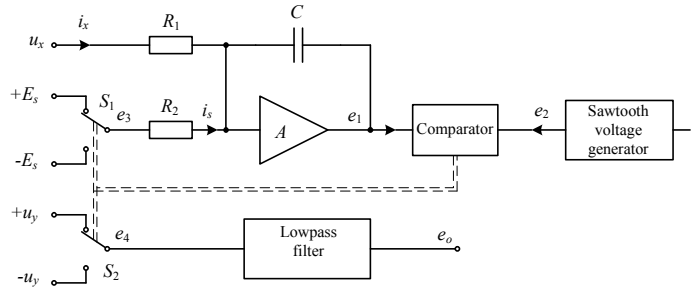
After the time t_2 voltage $e_1 > e_2$ and at the comparator output occurring state change causing switches S_1 and S_2 switching. On the switching inputs are respectively voltages $-E_s$ and $-u_y$. In the time interval t_1 voltage u_x forces current i_x, which charges the capacitor C, and voltage $-E_s$ induces current $-i_s$, which discharge the capacitor C. At these capacitor is voltage change given by the equation

$$\Delta u_c + \left[-\frac{1}{C}\int_o^{t_1}(i_x - i_s)dt\right] = 0, \tag{4.74}$$

hence

$$\Delta u_c = \frac{1}{C}\int_o^{t_1}\left(\frac{u_x}{R_1} - \frac{E_s}{R_2}\right)dt = \left(\frac{u_x}{R_1} - \frac{E_s}{R_2}\right)\frac{t_1}{C}. \qquad (4.75)$$

a)



b)

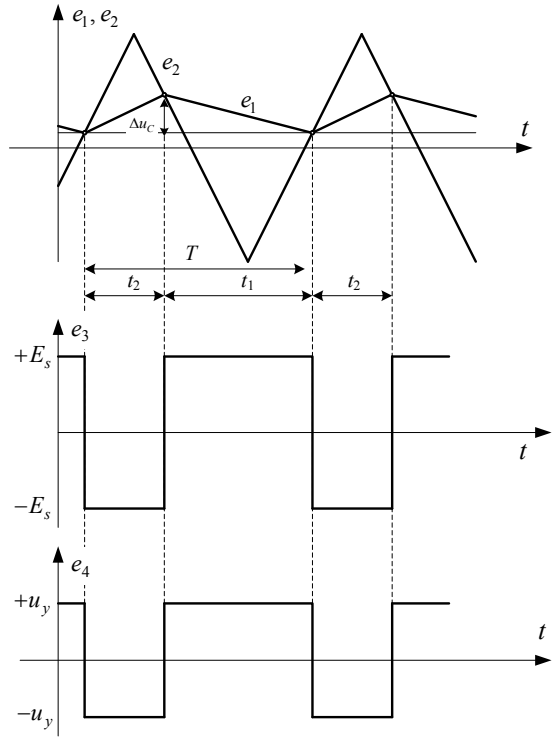


Fig. 4.25 TDM circuit
a) structural scheme b) voltage waveforms

From comparison of relations (4.73), (7.75) was obtained

$$\frac{u_x}{E_s}\cdot\frac{R_2}{R_1}=\frac{t_1-t_2}{t_1+t_2}=\frac{t_1-t_2}{T}. \tag{4.76}$$

Substituting the above expression into equation (4.69), which defines low-pass filter output voltage, obtained

$$e_o=-\frac{R_2}{R_1}\frac{u_x u_y}{E_s}. \tag{4.77}$$

Formula (4.77) indicates that the operation result is proportional to the product of the voltages u_x and u_y, and inversely proportional to the voltage E_s , and does not depend on the amplitude and frequency from the signal generator. A formula was derived under the assumption that the correct modulation condition is done ($f_gT<<1$).

TDM circuits form a class of analog multipliers with the highest accuracies. The disadvantage of this class of multipliers is limited by bandwidth multiplied signals and processed signals must be characterized by a low slew rate parameter. The dynamic properties of multipliers, except the above condition, depend on the speed of switching elements.

4.7. ERRORS OF SIGNALS MULTIPLICATION AND DIVISION

Errors of signals multiplication and division operations are determined by the properties of static and dynamic converters. The characteristic parameters of typical multiplier-divider are given in Table 4.4. The following will be given relations according to the static errors of multipliers and dividers

Table 4.4. Typical multiplier-dividers parameters [17]

Multiplication realization technique	Quadrature chatracteristic converter	TDM	Multipliers with controlled current division	Multipliers realizing logarithm and exponencial operations
Main terror related to 10V	0.25 ÷ 0,5%	0.01 ÷ 0,1%	0.2 ÷ 2%	0.1 ÷ 0,5%
Additional temperature error	0.03 %/° C	0.001 %/° C	0.01 %/° C	0.015 %/° C
Bandwidth (3 dB) for low signals	20 MHz	2 kHz	100 MHz	250 kHz
Slew rate	20 V/μs	1 V/μs	400 V/μs	1 V/μs
Additional information	High accuracy, wide bandwidth	Very good static properties, narrow bandwidth, expensive	Average accuracy, wide bandwidth, universal, cheap	High accuracy, average bandwidth, cheap

4.7.1. Multiplier static errors

Multiplier static errors depend on the calibration accuracy, the input voltage offset and linearity error. Consider the multiplier realizing operation

$$e_o = c\frac{u_x u_y}{10}, \tag{4.78}$$

where: c – multiplier constant, at the ideal multiplier $c = 1$.

Substituting to the above equation errors and their determinants for processing, one gets [13, 17]

$$e_o(1+\delta e_o) = c(1+\delta M)\frac{(u_x + X_{os})(u_y + Y_{os})}{10} + M_{os} + n(u_x, u_y), \tag{4.79}$$

where: δe_o – multiplier error,
δM – multiplier calibration error,
X_{os} – input offset voltage of line *x,*
Y_{os} – input offset voltage of line *y*,
M_{os} – multiplier output offset voltage,
$n(u_x, u_y)$ – multiplier linear errors depends on u_x^2 , u_y^2 , $u_x^2 u_y$, $u_x u_y^2$, etc.,

when $u_x = u_y = 0$ then $n(0,0) = 0$.

Dividing this expression by the relation (4.78) and omitting the secondary importance words obtained the processing system multiplier relative error

$$\delta e_o = \delta M + \frac{X_{os}}{u_x} + \frac{Y_{os}}{u_y} + 10\frac{M_{os}}{u_x u_y} + 10\frac{n(u_x, u_y)}{u_x u_y}. \tag{4.80}$$

This equation indicates the effect of calibration error, input and output offset voltage of a multiplier processing error. The multiplier output voltage taking into account processing errors were obtained by combining the expression (4.79) and (4.80)

$$e_o(1+\delta e_o) = c\frac{u_x u_y}{10}\left[1 + \delta M + \frac{X_{os}}{u_x} + \frac{Y_{os}}{u_y} + 10\frac{M_{os}}{u_x u_y} + 10\frac{n(u_x, u_y)}{u_x u_y}\right] \tag{4.81}$$

This equation also indicates the action procedure to enable improvement of the multiplier metrological properties. The sequence of steps to prepare multiplier for the work is as follows (see Fig. 4.26):

1. Minimize effect of M_{os} – the input terminals connected to ground (u_{x1}=u_{y1} = 0), The multiplier output voltage we are taking down to zero ($e_o(M_{os})$ = 0), with the nulling circuit attached to input *z*.

2. Minimize effect of X_{os} – input terminal x_1 shorted with ground, on the input y_1 we give voltage u_{y1} = 10 V and with nulling circuit connected to input x_2 we are taking down the output voltage to zero ($e_o(X_{os})$=0).
3. Minimize effect of Y_{os} – proceed as in the above point.
4. Multiplier callibration - on the inputs x_1 and y_1 we gives voltage u_{x1}=u_{y1}=10.000 V and changing the amplification of output stage so that the output voltage e_o=10.000 V.
5. This procedure, we repeat several times.

Today's circuits are calibrated and the multipliers are adjusted input and output offset voltage and for standard applications we do not need any correction systems. When are required better multipliers parameters, it is necessary to minimize the input and output offset voltage as shown in Fig. 4.26. for multiplier AD633 and calibrate it.

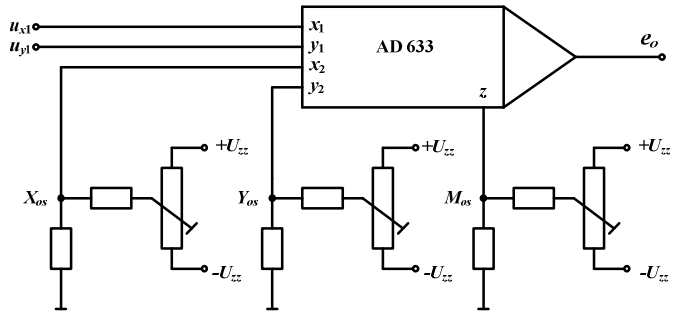


Fig. 4.26. Circuit for minimizing the effect of input and output offset voltages for AD633

4.7.2. Divider static errors

Divider realize operation

$$e_o = 10c\frac{u_x}{u_y}, \tag{4.82}$$

where: c – multiplier constant, at the ideal divider c = 1.

After substituting to the above equation quantities effects on divider processing, one gets

$$e_o\left(1+\delta e_o\right) = 10c\left(1+\delta M\right)\frac{u_x + X_{os}}{u_y + Y_{os}} + M_{os} + n\left(u_x, u_y\right). \tag{4.83}$$

Quantities effects on divider processing errors are discussed in the analysis of the multiplier. After dividing this expression by the relation (4.82) was obtained

$$\delta e_o = \delta M + \frac{X_{os}}{u_x} + \frac{Y_{os}}{u_y} + \frac{M_{os}}{10\dfrac{u_x}{u_y}} + \frac{n\left(u_x, u_y\right)}{10\dfrac{u_x}{u_y}}. \tag{4.84}$$

This equation indicates the divider error dependence on the calibration error and input offset voltage and indicates a the circuit preparation procedure to a division operation.

Joining equations (4.83) and (4.84), one gets

$$e_o\left(1+\delta e_o\right) = 10c\frac{u_x}{u_y}\left[1+\delta M + \frac{X_{os}}{u_x} + \frac{Y_{os}}{u_y} + \frac{M_{os}}{10\dfrac{u_x}{u_y}} + \frac{n\left(u_x, u_y\right)}{10\dfrac{u_x}{u_y}}\right], \tag{4.85}$$

which describes the divider output voltage.

4.8. DIVIDERS REALIZATION

Divider created from a multiplier-divider circuit

Multiplier-divider circuit described by processing function (look at the circuit shown in Fig. 4.11)

$$E_o = U_z\left(\frac{U_y}{U_x}\right)^{mn}, \tag{4.86}$$

realizing division operation, when input voltage U_z is equal to 10 V, and factor $m = n = 1$ (Fig. 4.27).

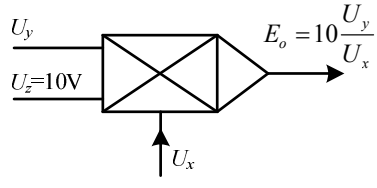


Fig. 4.27. Divider created from a multiplier-divider circuit

Then the division operations is

$$E_o = U_z\left(\frac{U_y}{U_x}\right) = 10\frac{U_y}{U_x}. \tag{4.87}$$

Divider created from multiplier and inverting amplifier

Idea scheme of that divider is presented in Fig. 4.28.

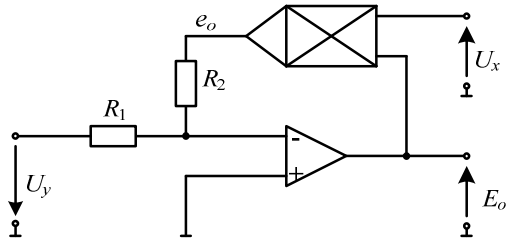


Fig. 4.28. Divider created from a multiplier and an inverting amplifier

If the voltage U_x and E_o are given on the multiplier inverting inputs, is to provide a negative feedback, the voltage U_y must have opposite polarity from the voltage U_x.

Analyzed circuit, assuming that the input offset voltage V_{os} is much higher than the operational amplifier differential voltage e_d, describing the equations

$$\begin{aligned} e_o &= \frac{E_o U_x}{10}, \\ \frac{e_o - V_{os}}{R_2} &= \frac{V_{os} - U_y}{R_1}. \end{aligned} \tag{4.88}$$

After transformations was obtained

$$E_o = -10\frac{U_y}{U_x}. \tag{4.89}$$

4.9. SQUARER REALIZATION

Squarer can be created from the multiplier-divider circuit and multi-functional operating circuit.

Squarer created from the multiplier-divider circuit

Multiplier-divider circuit realizing squaring operation is presented in Fig. 4.29. This circuit is described by relation

$$e_o = \frac{u_x u_y}{U_z}. \tag{4.90}$$

If the voltage U_z = 10 V, and $u_x = u_y$, then

$$e_o = \frac{u_x^2}{10}. \tag{4.91}$$

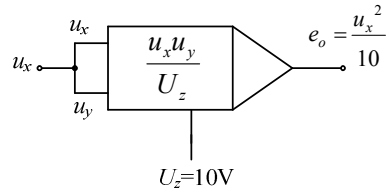


Fig. 4.29. Squarer created from the multiplier-divider circuit

Squarer created from multifunction operating circuit

The multifunction operating circuit realizing squaring operation is shown in Fig. 4.30

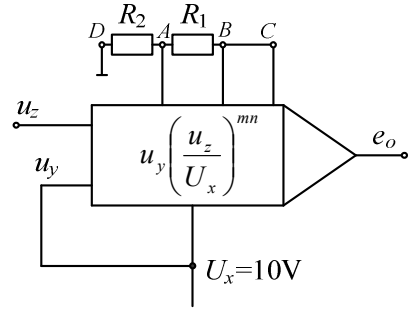


Fig. 4.30. Squarer created from the multifunction operating circuit

Multifunctional circuit output voltage is described by equation (4.39)

$$e_o = u_y\left(\frac{u_z}{U_x}\right)^{mn}, \tag{4.92}$$

where:

$$m = \frac{R_4}{R_3 + R_4}, \qquad n = \frac{R_1 + R_2}{R_2}.$$

If the following relation will be kept

$m = 1$, it is for $R_3 = 0$ and $R_4 = \infty$,

$n = 2$, it is for $R_1 = R_2$, and $U_x = u_y = 10$ V,

then the circuit will be realizing squaring operation in accordance to equation

$$e_o = 10\left(\frac{u_z}{10}\right)^2. \tag{4.93}$$

4.10. SQUARE ROOTERS REALIZATION

Square rooters can be created from the multiplier-divider circuit and multi-functional operating circuit.

Square rooter created from the multiplier and operational amplifier

Square rooter created from the multiplier and operational amplifier is presented in Fig. 4.31.

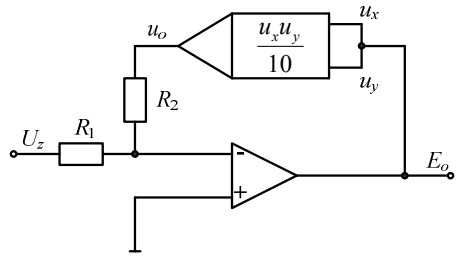


Fig. 4.31. Square rooter created from the multiplier and operational amplifier

Multiplier output voltage is described by expression

$$u_o = \frac{u_x u_y}{10} = \frac{E_o^2}{10}. \tag{4.94}$$

Through resistors R_1 and R_2 flowing currents determined assuming that the differential voltage is less than the amplifier input offset voltage

$$\frac{u_o - V_{os}}{R_2} = \frac{V_{os} - U_z}{R_1}. \tag{4.95}$$

After transformation above relations, one gets

$$E_o^2 = 10u_o, \tag{4.96}$$

$$u_o = \frac{R_2}{R_1}\left(V_{os} - U_z\right) + V_{os}. \tag{4.97}$$

Skipping an operational amplifier input offset voltage V_{os} and assuming, that $R_1 = R_2$ from equations () and () we obtain

$$E_o = \sqrt{-10E_z} \tag{4.98}$$

Square rooter created from the multiplier-divider

Multiplier-divider circuit realizing square rooting operations is shown in Fig. 4.32.

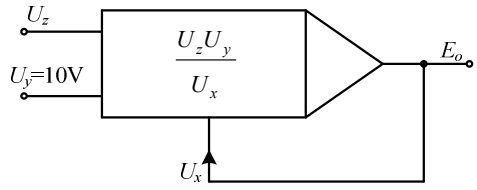


Fig. 4.32. Square rooter created from the multiplier-divider

Substituting to multiplier-divider processing equations described by equation (4.40)

$$U_y = 10 \text{ V}, \qquad U_x = E_o,$$

we obtained

$$E_o^2 = 10U_z . \tag{4.99}$$

Hence

$$E_o = \sqrt{10U_z} \tag{4.100}$$

Square rooter created from the multifunction operating circuit

Multi-function operating circuit realizing square-rooting operations is presented in Fig. 4.33.

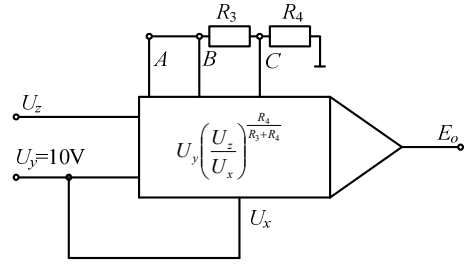


Fig. 4.33. Square rooter created from the multifunction operating circuit

Assuming, that resistors R_3 and R_4 have the same value, circuit is realized operation

$$E_o = 10\left(\frac{U_z}{10}\right)^{\frac{1}{2}} = \sqrt{10U_z} , \tag{4.101}$$

4.11. MAXIMUM, MEAN, AND RMS VOLTAGE VALUE CONVERTERS

Periodic signals are described by the following quantities:

- maximum value

$$U_m,$$

which for sine wave is an amplitude of this signal,

- mean value

$$\overline{u} = \frac{1}{T}\int_0^T u dt\,, \tag{4.102}$$

- rectified mean value

$$\overline{U} = \frac{1}{T}\int_o^T |u| dt\,, \tag{4.103}$$

- RMS value

$$U = \sqrt{\frac{1}{T}\int_0^T u^2 dt}\,. \tag{4.104}$$

In addition, to signals evaluation and metrological properties of converters are used:

- form factor

$$k_k = \frac{U}{\overline{U}}, \tag{4.105}$$

- crest factor

$$k_s = \frac{U_m}{U}. \tag{4.106}$$

4.11.1. Maximum value converters

Maximum value converters due to the conversion technique can be devided into:

- passive,
- active.

Fig. 4.34 shows a passive converter of the maximum positive half-wave, which depends on the diode parameters can be used in a wide frequency range [19, 30]

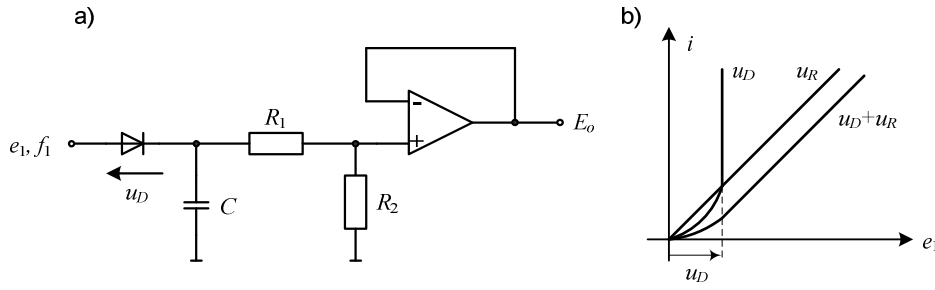


Fig. 4.34. Passive converter of the maximum positive half-wave
a) a converter scheme, b) the characteristic

When conditions are kept

$$e_1 >> u_D\,, \tag{4.107}$$

where: u_D – voltage drop on the diode

and

$$C(R_1 + R_2) >> \frac{1}{2\pi f_1}\,, \tag{4.108}$$

then the voltage drop on the diode may be omitted and assumed that the processing is realized on the linear part of the characteristic and the capacitor C discharge must be carried in accordance with a time constant $C(R_1+R_2)$.

Then, the converter processing the signal E_m maximum value of positive voltage half-wave e_1 into voltage E_o according to the formula

$$E_m = \frac{R_1 + R_2}{R_2} E_o\,. \tag{4.109}$$

Much better parameters characterizes the active converter of the maximum positive half-wave shown in Fig. 4.35.

In this circuit, the amplifier W_1 forces voltage on the capacitor C equal to the maximum voltage value e_1, because the differential voltage e_d of amplifier W_1 tends to zero value. The use of an amplifier W_1 with high gain causes that the output voltage of the amplifier W_1 during the diode D_1 conducting is higher than the voltage e_1 of the voltage drop u_D on this diode.

The converter is characterized by a high input resistance and has a very good metrological properties because two amplifiers are covered by the negative feedback loop. For the positive half-wave voltage, a negative feedback loop is covered amplifier W_2 operating in a voltage follower configuration and amplifier W_1, while for the negative half-wave, by negative feedback is covered amplifier W_1.

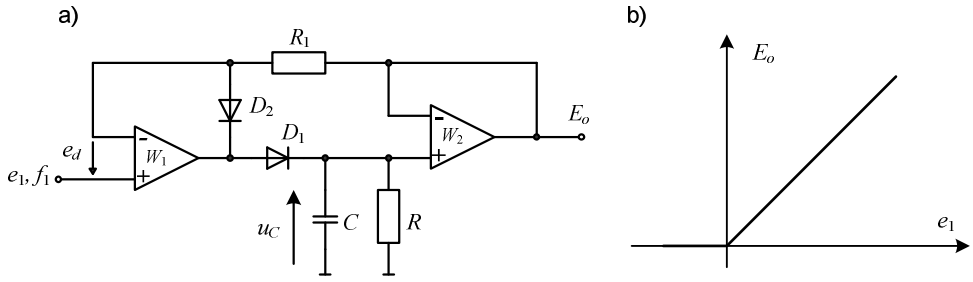


Fig. 4.35. Active converter of the maximum positive half-wave
a) a converter scheme, b) the characteristic

The converter is working properly when the condition is kept

$$RC >> \frac{1}{2\pi f_1}. \tag{4.110}$$

Processing statistical error of this converter is no higher than 0.1%. and practically depends on the used diodes D_1 and D_2 characteristics.

Błąd statyczny przetwarzania przetwornika nie przekracza 0,1% i praktycznie nie zależy od charakterystyk zastosowanych diod. Diodes residual parameters (capacitance, inductance) should be sufficiently low, because otherwise affect the high-frequency processing signal error.

In the electrical measurements technique are also used peak-peak (Pk-Pk) value converters. The simplest passive Pk-Pk converter is shown in Fig. 4.36.

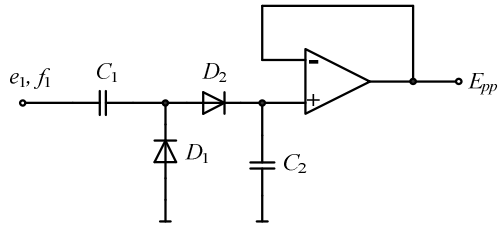


Fig. 4.36. Peak-peak value passive converter

This converter has similar properties as a passive maximum value converter. The circuit principle of operation is as follows, negative half-wave voltage e_1 causes the diode D_1 current, which charges capacitor C_1 to the approximate value of the voltage e_1. During the positive half-wave voltage, this voltage and the voltage on the capacitor C_1 accumulate and cause diode D_2 current, which charges capacitor C_2 to Pk-Pk voltage, which is then transferred to voltage follower.

Incomparably better metrological parameters has an active Pk-Pk value converter, which is formed of two active maximum value converters, positive and negative half-wave and signals adder amplifier. In case of use on the output the difference amplifier receives the signal as a difference of maximum value half-waves - positive and negative.

4.11.2. Mean value converter

For this class of converters the converter shown in Fig. 4.37 has a very good parameters. [19, 30].

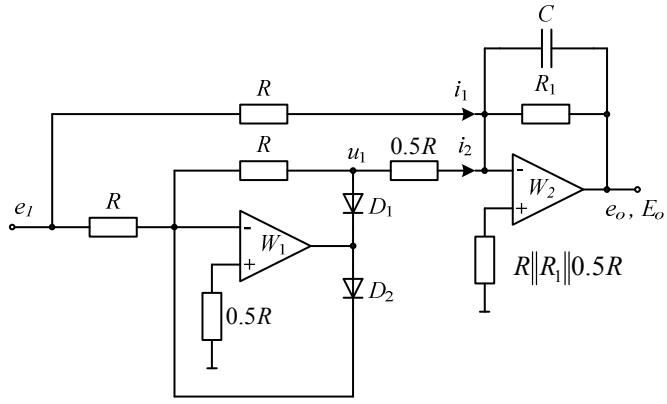


Fig. 4.37. Mean value converter

The converter due to its good metrological parameters is also called a linear charger. In the properly built converter the processing error caused by amplifier parameters is greater than the error caused by the diodes parameters [13, 17]. Converter principle of operation illustrate the voltage and current curves shown in Fig. 4.38.

Voltage u_1 behind diode D_1 is a inversion of positive half-wave voltage e_1. Diode D_1 junction voltage drop doesn't affect the processing signal u_1 because the amplifier W_1 forces current, which flows through the diode D_1, resistor R to the inverting input of amplifier W_1. This current is equal to the voltage source e_1 current which flows through a resistor R to the inverting input of the amplifier. The input voltage e_1 and received voltage u_1 are summed at the non-inverting amplifier W_2 input, and its output when the capacitor C is not connected, you get a rectified voltage e_o. Connection of capacitor C, with sufficiently large values of capacitance causes averaging e_o (no pulse), so that the amplifier W_2 output the voltage $\overline{E}_o$ is obtained.

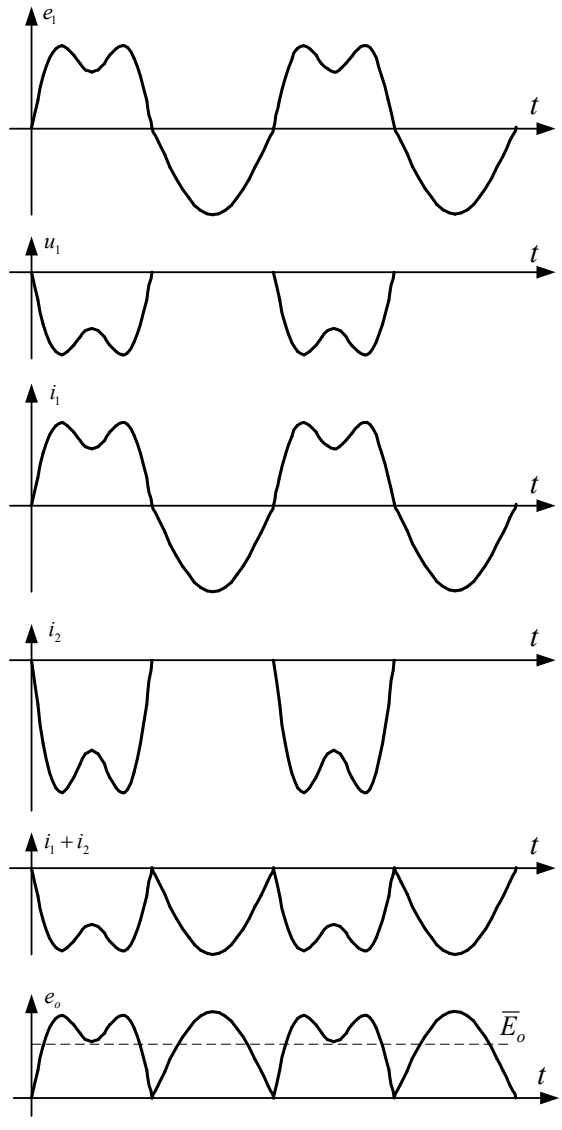


Fig. 4.38. Voltages and currents waveforms of the mean value converter

4.11.3. RMS value converters

Analog RMS converters are divided into two classes. One comprises non-feedback RMS converters and because of the function which describes them they are referred to as converters described by the explicit function. The other class includes feedback converters described by the implicit function. [8, 13, 17, 19].

RMS converter described by explicit function

The function circuit of an non-feedback RMS converter described by the explicit function is shown in Fig. 4.39.

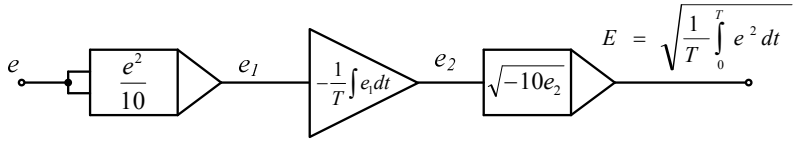


Fig. 4.39. The functional circuit of a RMS converter described by the explicit function

The converter consists of a squaring circuit, integrating circuit and square rooter. Metrological parameters are characterized by

- a squaring circuit described by the equation

$$e_1 = k_k\left(1+\delta k_k\right)\frac{\left(e+X\right)^2}{10}, \tag{4.111}$$

- an integrating circuit described by the relation

$$e_2 = -k_c\left(1+\delta k_c\right)\frac{1}{T}\int_0^T\left(e_1+Y\right)dt, \tag{4.112}$$

and a square rooter performing the operation

$$E = k_p\left(1+\delta k_p\right)\sqrt{-10\left(e_2+Z\right)}, \tag{4.113}$$

where:

e - the processed input signal;

e_1, e_2 - signals at the outputs of respectively the squaring circuit and the integrating circuit;

E - the signal at the square rooter circuit output, whose average value is proportional to the RMS value of input signal u;

k_k, k_c, k_p - the processing constants of respectively the squaring, integrating and rooter circuits;

$\delta k_k, \delta k_c, \delta k_p$ - processing constant errors of the circuits (multiplicative errors);

X, Y, Z - input offset voltages of the circuits (additive errors).

The processing constants, processing errors of the circuits and input offset voltages of above circuits are presented in section 4.7. Multiplicative errors causes processing constant value change - changing the gradient of the processing characteristics. Additive errors add up to the input signal - causing a parallel shift of processing characteristics.

Relations (4.111) and (4.112) were substituted into expression (4.113) and the following equation describing the processing by the RMS converter described by the explicit function was obtained

$$E = k_p\left(1+\delta k_p\right)\sqrt{10\left\{k_c\left(1+\delta k_c\right)\frac{1}{T}\int_o^T\left[k_k\left(1+\delta k_k\right)\frac{\left(e+X\right)^2}{10}+Y\right]dt+Z\right\}}\,. \quad (4.114)$$

Assuming that multiplicative and additive errors are time-independent and that e is a AC signal, after simplifications was obtained

$$E = k_p^2\left(1+\delta P\right)\sqrt{k_c k_k \frac{1}{T}\int_o^T e^2 dt}\,, \quad (4.115)$$

where δP_E stands for the convertor error given by the relation

$$\delta P = \delta k_p + \frac{1}{2}\left(\delta k_c + \delta k_k + \frac{X^2+10Y}{E^2} + \frac{10Z}{k_c k_k E^2}\right). \quad (4.116)$$

Assuming that processing constants $k_k = k_c = k_p = 1$, one gets

$$E = \sqrt{\frac{1}{T}\int_0^T u^2 dt}\left(1+\delta P_E\right), \quad (4.117)$$

$$\delta P_E = \sqrt{\delta k_p^2 + \frac{1}{4}\left(\delta k_c^2 + \delta k_k^2 + \frac{X^4+100(Y^2+Z^2)}{E^4}\right)}. \quad (4.118)$$

The last relation indicates that the processing error for low RMS values depends on the input offset voltages, offset voltages of integrating circuit and squaring circuit (Y, Z).

RMS CONVERTER DESCRIBED BY IMPLICIT FUNCTION

The function circuit of a feedback RMS converter described by the implicit function is shown in Fig. 4.40.

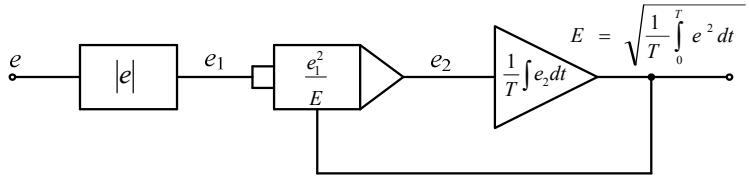


Fig. 4.40. The function circuit of a RMS converter described by the implicit function.

The converter consists of an absolute value circuit, a multiplier-divider and an integrating circuit.

General principle of converter operation is as following. The multiplier-divider output voltage described by the equation

$$e_2 = \frac{e_1^2}{E} = \frac{e^2}{E}, \tag{4.119}$$

which after integrating, one gets

$$\frac{1}{T}\int_o^T \frac{e^2}{E} dt = E \tag{4.120}$$

And is described by implicit function (unknown appears on both sides of the equation). Since the voltage E is a fixed value, the converter output voltage is equal

$$E = \sqrt{\frac{1}{T}\int_o^T e^2 dt}\,. \tag{4.121}$$

Below the metrological analysis of converter is presented.

Metrological parameters are characterized by relations:

- an absolute value circuit described by the equation

$$e_1 = k_b(1+\delta k_b)(|e| + X), \tag{4.122}$$

- a multiplier-divider performing mathematical operations in the first quadrant of a rectangular coordinate system

$$e_2 = k_F(1+\delta k_F)\frac{(e_1+Y)^2}{E+Z}, \tag{4.123}$$

- an integrating circuit described by the equation

$$E = k_c(1+\delta k_c)\frac{1}{T}\int_o^T (e_2 + W)dt, \tag{4.124}$$

where:

u - the processed input signal;

e_1, e_2 - signals at the outputs of respectively the absolute value circuit and the multiplier/divider;

E - the signal at the output of the rooter, whose average value is proportional to the RMS value of input signal u;

k_b, k_c, k_F - the processing constants of respectively the absolute value circuit, the integrating circuit and the multiplier/divider;

$\delta k_b, \delta k_c, \delta k_F$ - circuit processing constant errors (multiplicative errors);

X, Y, Z, W - input circuit offset voltages (additive errors).

Having substituted relations (4.122) and (4.123) into expression (4.124) and after simple transformation the following was obtained

$$E = k_c(1+\delta k_c)\frac{1}{T}\int_o^T \left[k_F(1+\delta k_F)\frac{k_b^2(1+2\delta k_b)^2(|e|+X)^2 + 2k_b(1+\delta k_b)(|e|+X)Y + Y^2}{E+Z} + W \right] dt. \quad (4.125)$$

After transformations, assuming that the voltage e is a sine wave and processing constants $k_F = k_c = k_b = 1$, the following is obtained

$$E = \sqrt{\frac{1}{T}\int_0^T u^2 dt}\,(1+\delta P_I), \quad (4.126)$$

where processing error δP_I is given by

$$\delta P_I = \sqrt{\frac{1}{4}\left[\delta k_c^2 + \delta k_F^2 + 4\delta k_b^2 + \frac{Z^2 + W^2 + \frac{4}{FF^2}\left(X^2+Y^2\right)}{E^2} + \frac{\left(X^2+Y^2\right)^2}{E^4} \right]}. \quad (4.127)$$

The analyzed converter for signals with small values processing the additive errors have a lesser affect on the processing error, rather than in the converter described by explicit function because additive errors occurring in the counters have the same exponent as the output voltage *E* in the denominators.

Table 4.5. Parameters of RMS converters

Converter	R 301	R 310	AD 536	AD 637
Processing error	± 0,1% ± 0,02% / ° C	± 0,05% ± 0,01% / ° C	± 0,2% ± 0,002% / ° C	± 0,05% ± 0,001% / ° C
Output offset voltage V_{OSO}	5 mV	5 mV	1 mV	0.5 mV
Input voltage U_{ZZ}= ± 15V Period curves U Pulse curves u_{pp}	0....7 V 20 V	0....7 V 20 V	0....7 V 20 V	0....7 V 15 V
1V RMS square wave processing error, and form factor depends on the pulse-width	a) ± 60 mV, k_S=3 ±200 mV, k_S=8	a) ± 60 mV, k_S=3 ±200 mV, k_S=8	± 0.1%, k_S=3 ± 1%, k_S=7	± 0.1%, k_S=3 ± 1%, k_S=10
bandwidth (error 1%) Voltage	100 kHz, U_{pp} < 2 V 1 MHz, U_{pp} < 20 V	100 kHz, U_{pp} < 2 V 1 MHz, U_{pp} < 20 V	45 kHz, U_{pp} > 0.1 V 120 kHz, U_{pp} <20 V	66 kHz, U_{pp}>0.2 V 200 kHz, U_{pp}<2 V

a) – the value of reference voltage and how to determine the absolute error are not given.

Table 4.5 presents the parameters of RMS converters. Converters R501 and R502 manufactured by Intronics are described by explicit function, converters AD 536 and AD 637 manufactured by Analog Devices are described by implicit function.

Example

Determine processing error of RMS converters described by explicit and implicit functions for sinusoidal signals with values ranging from 0.01 V to 10 V.

Processing constant errors and output offset voltages are equal

$$\delta k = \delta k_k = \delta k_c = \delta k_p = \delta k_F = \delta k_b = \pm 0.1\%$$

$$X = Y = Z = W = \pm 0.5\text{mV}$$

Equations (4.118), (4.127) for data presented in this example gets

$$\delta P_E = 2\delta k + \frac{10X + \frac{1}{2}X^2}{E^2} \approx 2\delta k + \frac{10X}{E^2},$$

$$\delta P_I = 2\delta k + \frac{X\left(1 + \frac{4\sqrt{2}}{\pi}\right)}{E} + \frac{2X^2}{E^2}.$$

For large values of E=10 V the processing errors depends on multiplicative processing errors

$$\delta P_E = \delta P_I = 2\delta k .$$

However, for small values of E at the processing errors affects only the input offset voltage (an additive error). Converters errors curves is shown in Fig. 4.41.

Carried out a comparative metrological analysis indicates that, for signals with smaller values of these parameters incomparably better are a RMS converters described by implicit functions, because mathematical operations performed inside the converters are done on the much larger values of the signals.

Previously was built converters described by explicit function. For large voltages have processing errors at 0.5 % or even 0.05 %. Significant developments in technology enabled the realization of mathematical operations using logarithmic and exponential functions. In these circuits is a natural process carried out in accordance with the description of the implicit function.

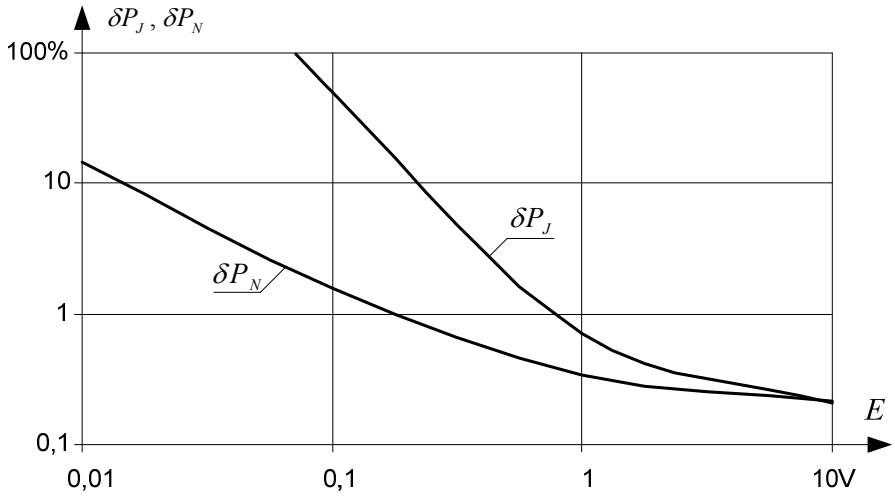


Fig. 4.41. Errors of RMS converters described by explicit and implicit function determined for $\delta k = \pm 0.1$ % and $X = \pm$ 0.5 mV

Dynamical properties of RMS converters : errors for low and high frequencies, slew rates is presented in [17].

PART II

Digital measurement systems

5. DIGITAL MEASUREMENT SYSTEM - GENERAL INFORMATION

The digital measurement system (DMS) can be classified as a set of technical means subordinated to the common goal of action, which is receiving information from the object, processing them according to the set algorithm, sending results, visualization and the archiving. Measuring instruments and additional devices, as well as software, both system and specialized, are being numbered among technical means.

5.1. CLASSIFICATION, STRUCTURE AND ORGANIZATION OF DIGITAL MEASUREMENT SYSTEMS.

A structure and organization of digital measuring systems depends on its application methods, measurement information processing rate etc. The basic structure of DMS is shown in Fig. 5.1.

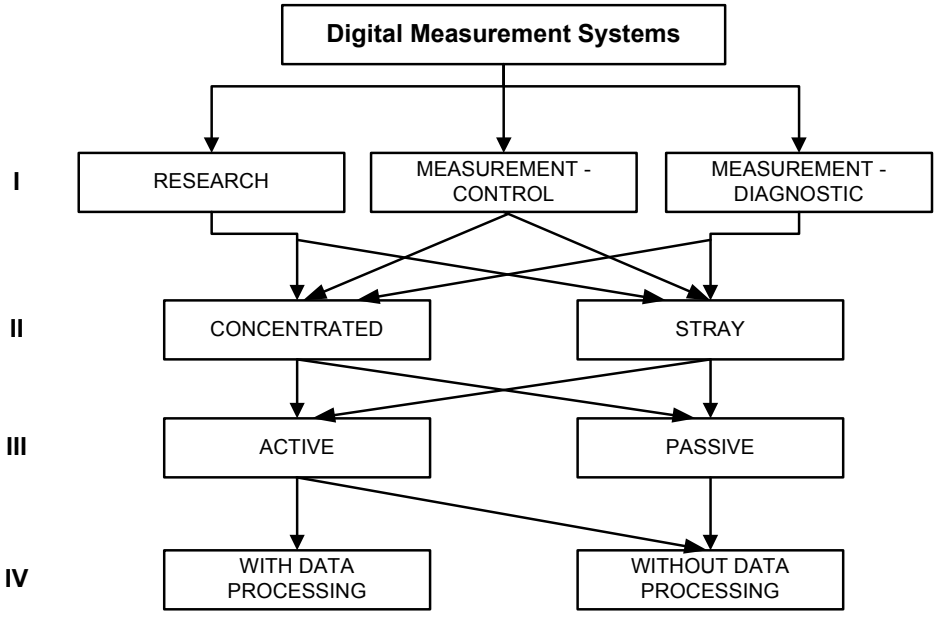


Fig. 5.1. A basic structure of a digital measurement system

The first level (I) of the diagram presents DMS division into the three main groups:

- *research measurement systems* are used in many science fields like physics, chemistry, electrical engineering, electronics, mechanics, medicine. These systems are the most extended, because they are usually used as a base for prototypes constructing.

- *control measurement systems* are usually used as integral part of every technological process in industry. Many kinds of sensors and conditioners are designed for this systems (spatially arranged on the object), which measurement signal are used by regulators responsible for technological process control. They are less complicated than research systems, but in this kind of systems user must have possibility to change some parts of the systems (for new model of data acquisition (DAQ) card, faster devices) and add a few new modules to the systems. The main user of this systems is the industry.
- *diagnostic measurement systems* are used for detection, localization and identification of object failures based on selective parameters measures. The diagnostic target is the estimation of object condition and indication of damaged element in the object. These systems are intended for specific devices and usually it's not possible to change anything at hardware, but it is possible to change the software. These systems are characterized by very low costs.

Each of this systems can be realized as concentrated, in one or few close to each other rooms, or stray (II). The third level (III) shows that some systems can be active (with interaction to the object) or passive (without interaction to the object), where user cannot do any data processing because in this systems the computer does not exist (IV). Active systems have computers (PC or specialized industry units) in the measuring line, so it is possibility to do data processing in real time (fast algorithms, fast processors) or in it is own time (extended algorithms).

General structure of a digital measurement system is presented in Fig. 5.2. [32]

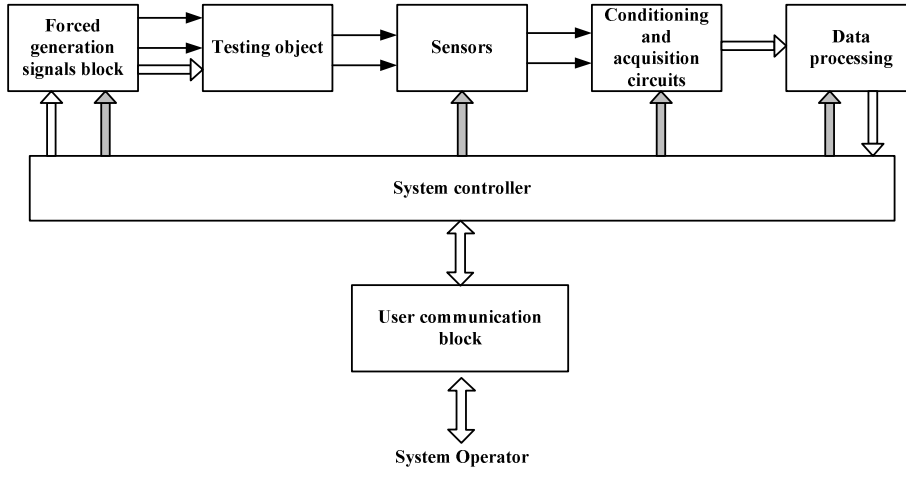


Fig. 5.2. A structure of a digital measurement system

In the chapter 5.2 each of presented blocks is discussed.

Organization of DMS relies on adequate transmission of information in measuring system. It is necessary to solve the following problems:

- choose the system configuration,
- choose the transmission method,
- provide correction of transmission.

Configuration of the measuring system is made in the functional blocks and the connection method is made in the measurement system. Information transfer is realized by two types of signals: information and organization.

Information signals (white arrows) carry details about measured quantity and conditions of measurement instruments. Organization signals (grey arrows) such as addresses, control signals, condition signals are necessary for correct system operation according to the algorithm assumptions.

In use there are four basis configurations of a measurement systems: sequential, star-shaped, linear (main line), loop and their combinations [32].

In the sequential configuration of a measurement system, which is presented in Fig. 5.3, the information signals are processed by every functional block (FB). Organization signals are connected between system controller and each of the functional blocks.

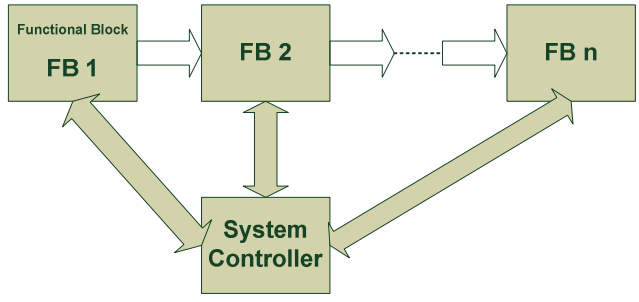


Fig. 5.3. Sequential configuration of a measurement system

The star configuration, where central position is reserved to system controller, is presented in Fig. 5.4. Each type of information in this configuration is transmitted between a controller and the separate functional block. Because every information could be processed only by a system controller this configuration is used only in a basic measurement systems, consisting of a few FB.

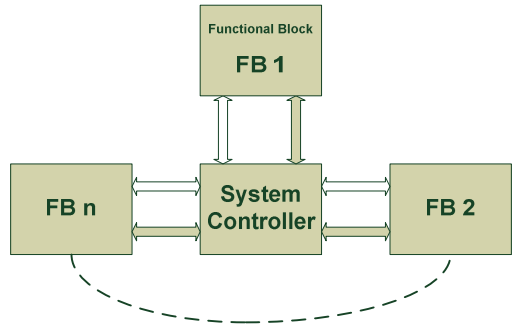


Fig. 5.4. The star configuration of a measurement system

The linear configuration or main line configuration of a measurement system is presented in Fig. 5.5. In this configuration all devices are connected in parallel to the digital main line. Each of connected devices can work as the system controller, but the device has to have potential to control the measurement system.

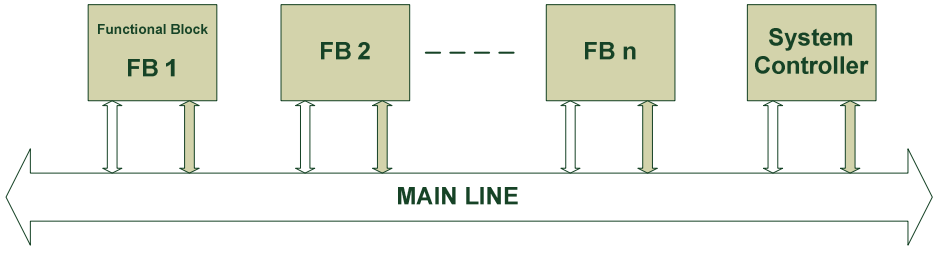


Fig. 5.5. The linear configuration of a measurement system

It is a very useful configuration, because user can divide the measurement processes to a few system parts and each of these parts can have specialized system controller. At time t_0 all of the receivers, but only one transmitter, can be activated. This configuration is characterized by possibility to change and expand the system when it is working.

The loop configuration is presented in Fig. 5.6. All signal lines are one way only lines, so the systems built with this configuration are characterized by low working speeds.

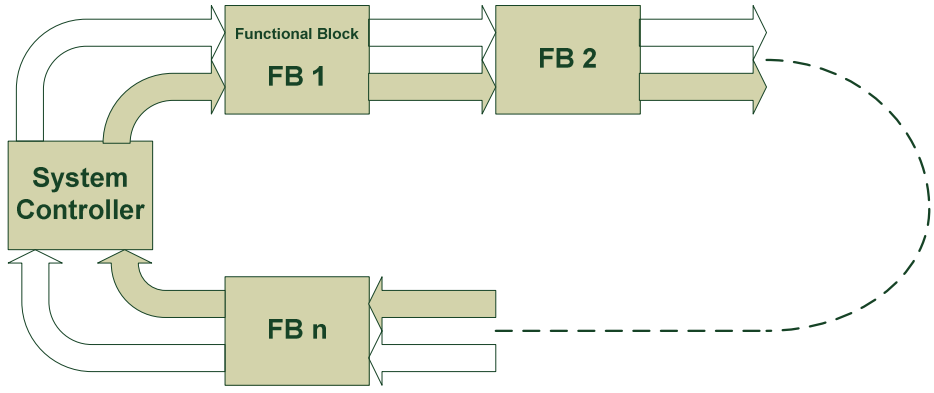


Fig. 5.6. The loop configuration of a measurement system

To sum up: the system configurations depends on complication of measuring algorithm, used measurement devices and software.

The next problem to solve is choosing the transmission set. It is dependent on two main factors:

- transmission distance,
- information transfer rate.

Information can be transferred by serial, parallel or serial – parallel interfaces. For low distances, usually the parallel transmission is used (for example GPIB interface) , because it provides high speed transmission. When user has to transfer the information on long distances then usually the serial transmission system is used (for example USB, LAN). Sometimes system users or designers can use serial – parallel configuration. Then it is possible to send measurement information between devices with high speed transmission and then send the results on a long distance.

Every information has to be transferred between devices and between devices and controller correctly. For sending correct information there can be used two basic transmission information time coordinated methods:

- synchronous data transmission

In this kind of transmission continuous streams of measured data signals are accompanied by signals generated by a clock to ensure that the transmitter and the receiver are synchronized with each other. The data is sent in blocks (called frames or packets) spaced by fixed time intervals. The packets also have end frames to indicate the end of the packet. The basic scheme of synchronous data transmission is shown in Fig. 5.7. Most network protocols, like the Ethernet and TokenRing, use the synchronous transmission.

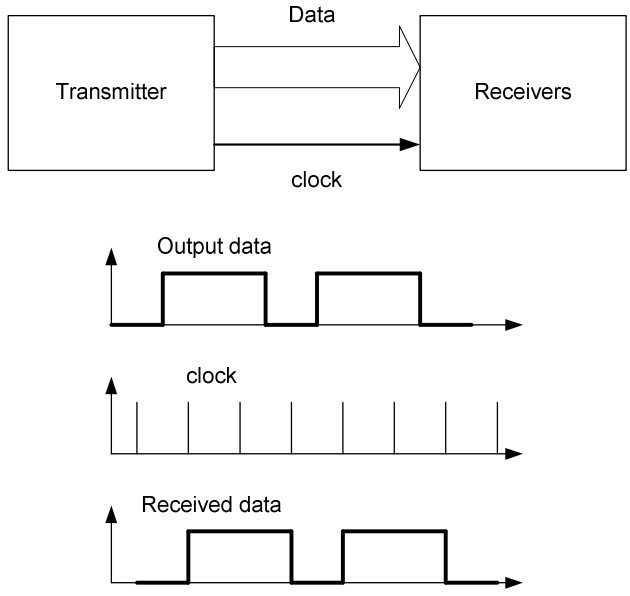


Fig. 5.7. Communication between the transmitter and the receiver with synchronous data transmission

- asynchronous transmission Fig. 5.8.

Asynchronous transmission works in waves. That is why it has to insert a start bit before each data character and a stop bit at its termination, to inform the receiver where the transmission begins and ends. This situation is presented in Fig. 5.8. Asynchronous transmission is used for communication over the telephone lines.

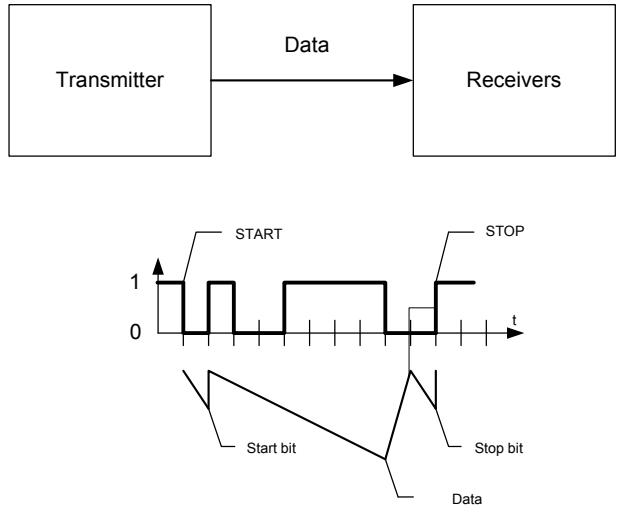


Fig. 5.8. Data communication with asynchronous data transmission

5.2. FUNCTIONAL BLOCKS OF DIGITAL MEASURING SYSTEMS

5.2.1. A controller

Controller it is a device in the measurement system responsible for realization of system operation algorithm [24, 28]. All operating instructions are located in the system memory. The control and operating instructions consist of:

- space – time coordinating system operation,
- determination of measurement condition,
- organization of all information in the transmission.

There can occur controllers with constant measurement algorithm (Siemens controllers series) and controllers with variable measurement algorithms (digital signal processors).

Processors used in automation measurement processes can be divided into three main groups:

- microprocessors (standard, RISC),
- microcontrollers (4, 8, 16, 32, 64 bits), in this there are the measurement oriented processors (with analog to digital A/D converters, D/A converters on board),
- signal processors.

The processors general functions in a measurement system are:

- control devices (power supplies, generators) and instruments (multimeters),
- collecting and storing of the measurement data,
- measurement data processing.

5.2.2. User communication block

System operator should have a possibility to communicate with the measurement system. It can be realized by using a controller and additional devices. To insert data to the system the switches can be used (when system is working without computer) or a keyboard, mouse and disk in computer aided systems. Output information could be realized by analog or digital recorders or by monitors.

5.2.3. A measurement data acquisition block

A measurement data acquisition block gives possibility to connect sensors and the data processing block. Its main task is the measurement data collection and its discretisation.

In this block there are carried out the following operations of measurement processes:

- signal conditioning – normalization of analog signals: voltage dividers, amplifiers, current to voltage converters,
- voltage to digital processing, time to digital processing.

Voltage to digital processing is used when the voltage is the indirect quantity: resistance, voltage, current. Time to digit processing is used when the time is the indirect quantity: frequency, time delay, phase shift, period.

In measurement systems very often there is a necessity of measurement of many physical quantities. The data acquisition can be done in a sequential sampling circuit or in a simultaneous sampling circuit. The basic structures of data acquisition blocks is presented in Fig. 5.9.

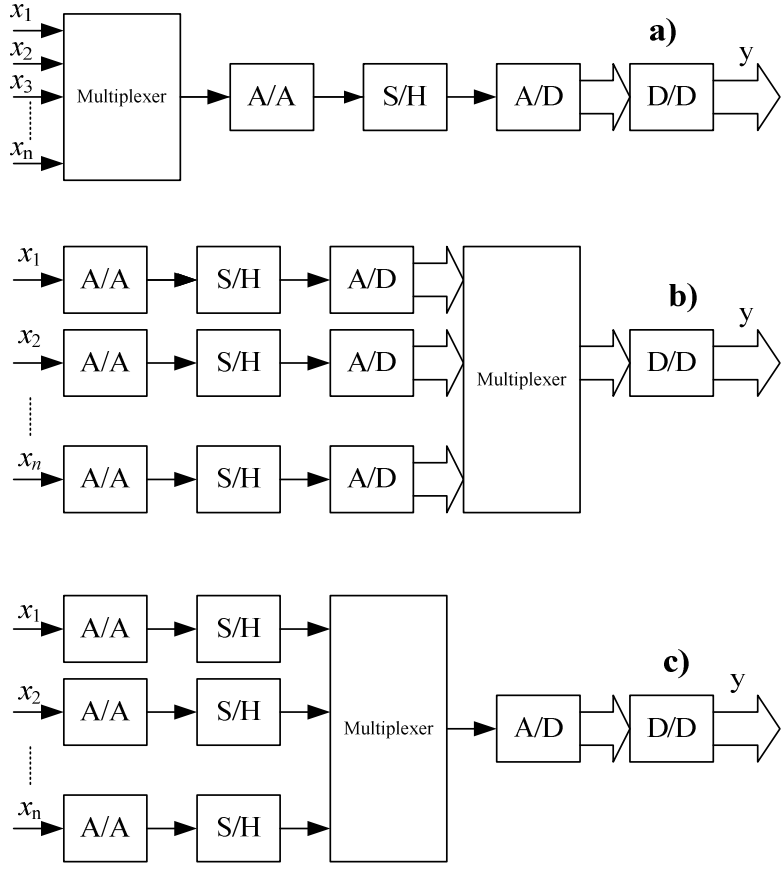


Fig. 5.9. A Data acquisition block a) with sequential sampling, b), c) simultaneous sampling, A/A – an analog to analog converter, S/H – a sample and hold circuit, A/D – an analog to digital converter, D/D – a digital to digital converter

This block consists of an input analog to analog converter, a sample and hold circuit, an analog to digital converter and an output digital to digital converter. The

multiplexer collects analog or digital data from sensors according to a specific algorithm. An A/A converter is used for conditioning signals from sensors. In this block there can be used: amplifiers, logarithmic circuits, integrators, low pass filters. A sample and hold operation is sequentially performed on each signal. Each of the sensor outputs is synchronously sampled and held before an A/D conversion, where the conversion of an analogue normalized signal to a digital code is realized. A D/D converter is allowing the digital signal match the system characteristics of data processing block.

Data acquisition lines consist of:

- conditioners,
- multiplexers,
- a sample and hold circuits,
- A/D converters,
- filters (analogue – low pass filters, digital – IIR, FIR, antialiasing filters).

To the main tasks of conditioners we can give:

- sensor output signal match to A/D converter input range,
- galvanic isolation guarantee.

A model of conditioner position in a measurement system is shown in Fig. 5.10.

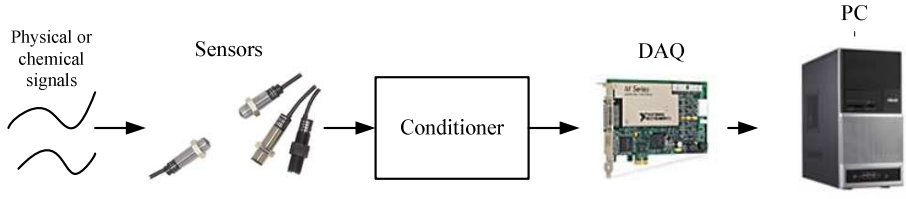


Fig. 5.10. A basis scheme of a digital measurement system.

Signal conditioning circuits have the following processing functions:

- signal scale processing (value),
- signal nature processing (quantity),
- signal shape processing (time wave).

To the signal scale processing systems we can assign: voltage dividers, amplifiers, presented in the first part of this book and instrument transformers. To signal nature processing we can assign: current to voltage converters, resistance to voltage converters, voltage followers. To signal shape processing there can be assigned the following circuits: comparators, filters and other shaping circuits.

Comment:

A measurement information in the processing time cannot be distorted when it is transformed between an individual steps of a measuring line.

Other functions of conditioners:

- a forced signal generation (current and voltage sources uses to control and supply other devices, for example measuring bridges),
- a characteristics linearization. Some kinds of converters cannot be used directly in measurement system because are characterized by high nonlinearity of characteristic.

Signal multiplexing is essential in an advanced measuring systems with many sensors. Multiplexer, as it is shown in Fig. 5.11, is a switching circuit with k information (signal) inputs, n addressing (control) inputs (usually $k = 2^n$) and one y output.

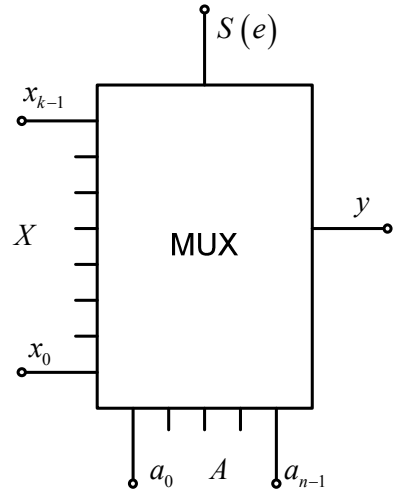


Fig. 5.11. A basis scheme of a multiplexer

Multiplexers consists of a control input too, named by Strobe (S) or Enable (e) which can control the circuit activity. Effect of this circuit is connection of one of the x_i inputs to y output. Input number i is described by addressing lines A. If on S (e) input is given a logical zero then the y output has concrete logical state (usually zero), independent of X and A input states.

Often before multiplexer in measurement line there is used a sample and hold (S/H) circuit. The sample of usage of this circuit is presented in Fig. 5.12.

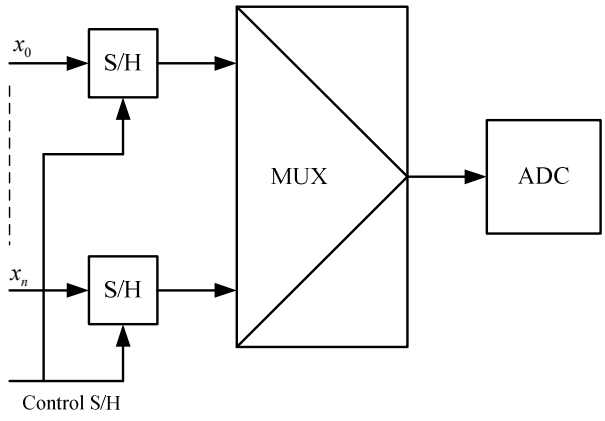


Fig. 5.12. Principle of use of a S/H circuit in measuring line

The basis configuration of S/H circuit is presented in Fig. 5.13

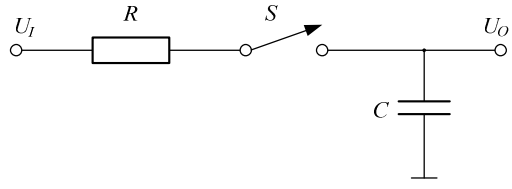


Fig. 5.13. A sample and hold circuit

Capacitor is used to store the analog voltage, and an electronic switch *S* is used to alternately connect and disconnect the capacitor from the analog input. In a sample and hold circuit the switch opens for a very short time duration.

Principle of operation:

The voltage input signal U_I flowing through resistor *R* and capacitor *C* is integrated when the switch *S* is closed. It is the time when the input signal is sampled. When the switch *S* is closed then the signal is remembered by the capacitor at time t_0.

Low signal transmission band is described by relation

$$f_{-3dB} = \frac{1}{2\pi RC} \tag{5.1}$$

and the maximum value of current is expressed by following equation

$$I_{\max} = \frac{U_{\max}}{R}. \tag{5.2}$$

A practical solution for a S/H with feedback is presented in Fig. 5.14.

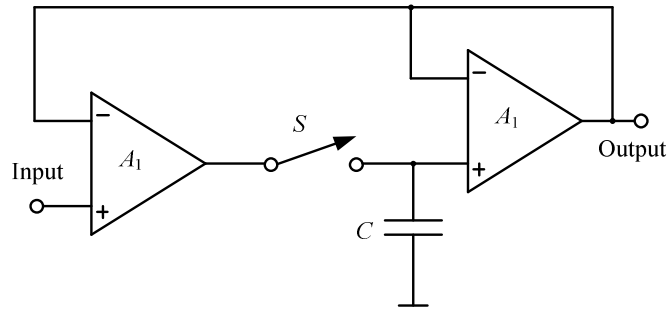


Fig. 5.14. A practical solution for a sample and hold circuit

There are four groups of specification that describe the basic S/H operation: sample mode, sample-to-hold transition, hold mode, hold-to-sample transition. These specifications are summarized in Table 5.2 , and some of the S/H error sources are shown graphically in Fig. 5.15. [33, 7]

Table 5.2. Specifications of Sample and Hold operations

Sample mode	Sample to Hold transition	Hold mode	Hold to Sample transition
Static: offset gain error nonlinearity	Static: pedestal pedestal nonlinearity	Static: droop dielectric absorption	Static:
Dynamic: setting time bandwidth slew rate distortion noise	Dynamic: aperture delay time aperture jitter switching transcient settling time	Dynamic: feedthrough distortion noice	Dynamic: acquisition time switching trancient

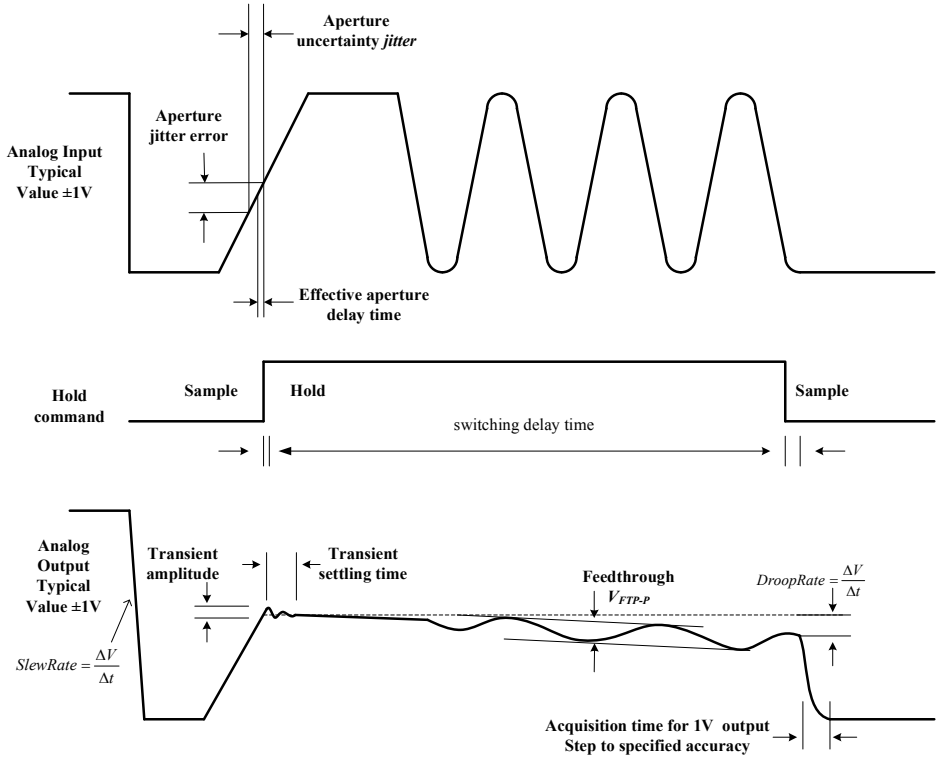


Fig. 5.15. Some sources of sample and hold errors

The DC offset voltage in a hold mode, which is called the *pedestal* error, is shown in Fig. 5.16. If the S/H is driving an A/D converter, the pedestal error appears as a DC offset voltage, which may be removed by performing a system calibration. Pedestal errors may be reduced by increasing the value of the hold capacitor, with a corresponding increase in acquisition time and a reduction in bandwidth and slew rate.

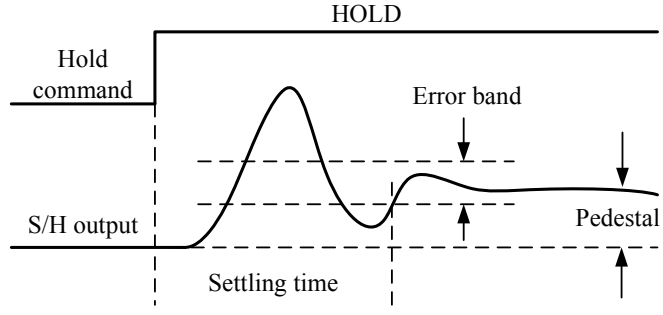


Fig. 5.16. The pedestal error

Data acquisition blocks can consist in basic form of multimeter with a standard interface. For example voltmeters with sampling A/D converter gives faster measuring signals, but with worse accuracy. When the user needs high accuracy, then he should choose the voltmeter with integrating A/D converter, which is characterized by low speed operation, but higher accuracy. Data acquisition blocks are developed as data acquisition cards (DAQ) with PC interfaces (PCI, PCIe, older ISA) or industrial specialized interfaces (PXI, PXIe, VXI, other). These DAQ cards installed in a PC or an industrial computer guarantee analog data collecting with a defined accuracy.

5.2.4. A data processing block

This block provides digital measuring signal processing according to an accepted measurement algorithm. Almost always, especially in modern systems, data operations are done in PC class computers, which also have controller functions. For small systems with a few measurement devices we can use a basic configuration of computer system. In advanced measurement systems we have to use modern multicore processors. Sometimes it is necessary to use special, additional blocks with signal processors. Then the user can design the real time measurement system with mathematically complicated data processing algorithms.

5.2.5. A signal generation block

The following signals generation are possible in this block:

- forcing signals (programmable sources),
- reference signals (standard signals),
- physical (real) object performance elements control

and to present measurement results in analog form. This block acts as an inverse function to data acquisition block.

6. A/D AND D/A CONVERTERS

6.1. INTRODUCTION

The analog signal is sampled at discrete intervals with sampling frequency f_s so that the information included in analog signal must be well-known on the converter output. The more the samples are taken, the more accurate the digital representation of input signal is. If fewer samples are taken, the information about analog signal can be lost. The mathematical basis of sampling theory was presented by H. Nyquist in 1924. The Nyquist criteria requires that the sampling frequency should be minimum twice the highest frequency contained in analog signal, which information can be used and analyzed after conversion. A signal with component of maximum frequency fmax must be sampled at a rate

$$f_s > 2 f_{\max} . \tag{6.1}$$

When relation (6.1) is not complied, then the information about signal will be lost and the aliasing occurs. Fig. 6.1 presents the case of time domain representation of a sine wave single tone sampled. The sampling frequency is slightly more than the analog input frequency $f_{\max}$ so the Nyquist criteria is not fully kept.

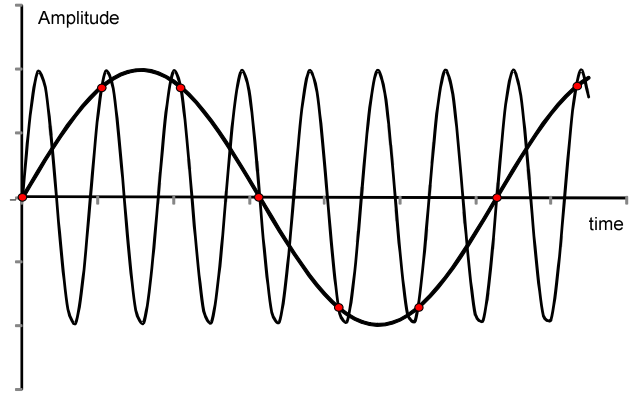


Fig. 6.1. Aliasing in the time domain

Fig. 6.2a presents the process of A/D conversion with analog filter [10].

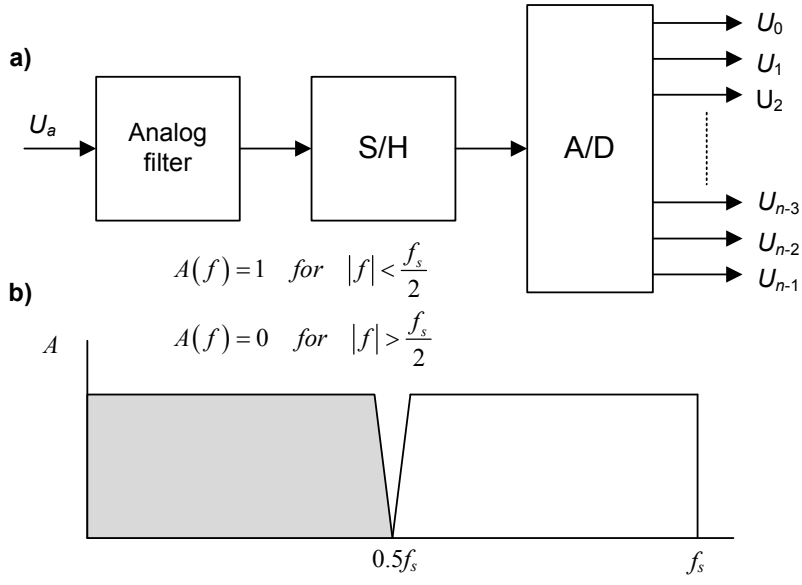


Fig. 6.2. A/D processing with analog filtration
a) a scheme, b) the characteristic

The grey area on the characteristic defines frequency response of an ideal low-pass filter. In the literature it is often named the passband. The half sample frequency neighbourhood area is called characteristic transient area (transient band) of practical (real) analog filter circuit. In this system the attention should be called on filter elements parameters: resistance, inductivity (should be wounded on large cases to avoid the core magnetise effects) and capacitance (only high quality capacitors). Moreover, the call attention, that usually the filter grade, is relatively high.

A/D processing with uses of both: analog and digital filters is presented in Fig. 6.3a. [10].

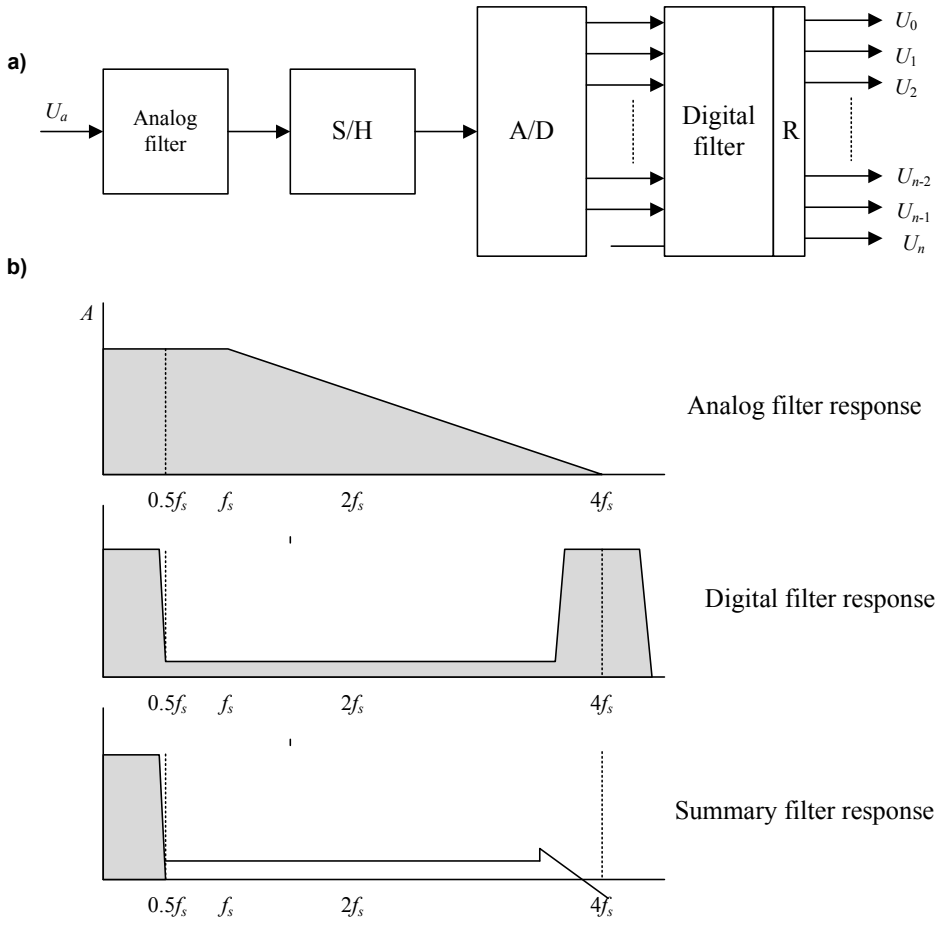


Fig. 6.3. A/D processing with analog and digital filtration
a) a scheme, b) the characteristics

In this system the A/D converter with four times oversampling makes possible to use simpler analog filter with almost linear phase characteristic, which is enough to attenuate signals around $4f_s$ frequency occurring. The digital filter has a steep passband characteristic, with 0.5 f_s band. Input signals which are between 3.5 and 4.5f_s interval must be filtered by analog filter. Analog filter attenuation in this area should be so high that overlay frequencies are smaller than quantization errors [10]. Summary attention should be thet large, that the decimation (subsampling) can be held without aliasing effects. The letter R signify decimate operation with ratio 4. The final result is a very exact filtration, with almost linear phase characteristic.

Inverse process is shown in Fig. 6.4 and 6.5 where the D/A conversion is done.

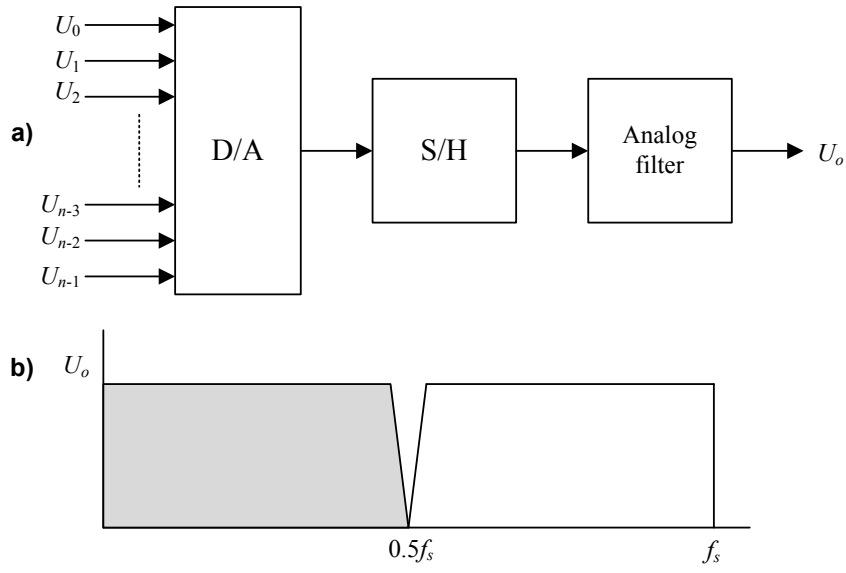


Fig. 6.4. D/A processing with analog filtration
a) a scheme, b) the characteristic

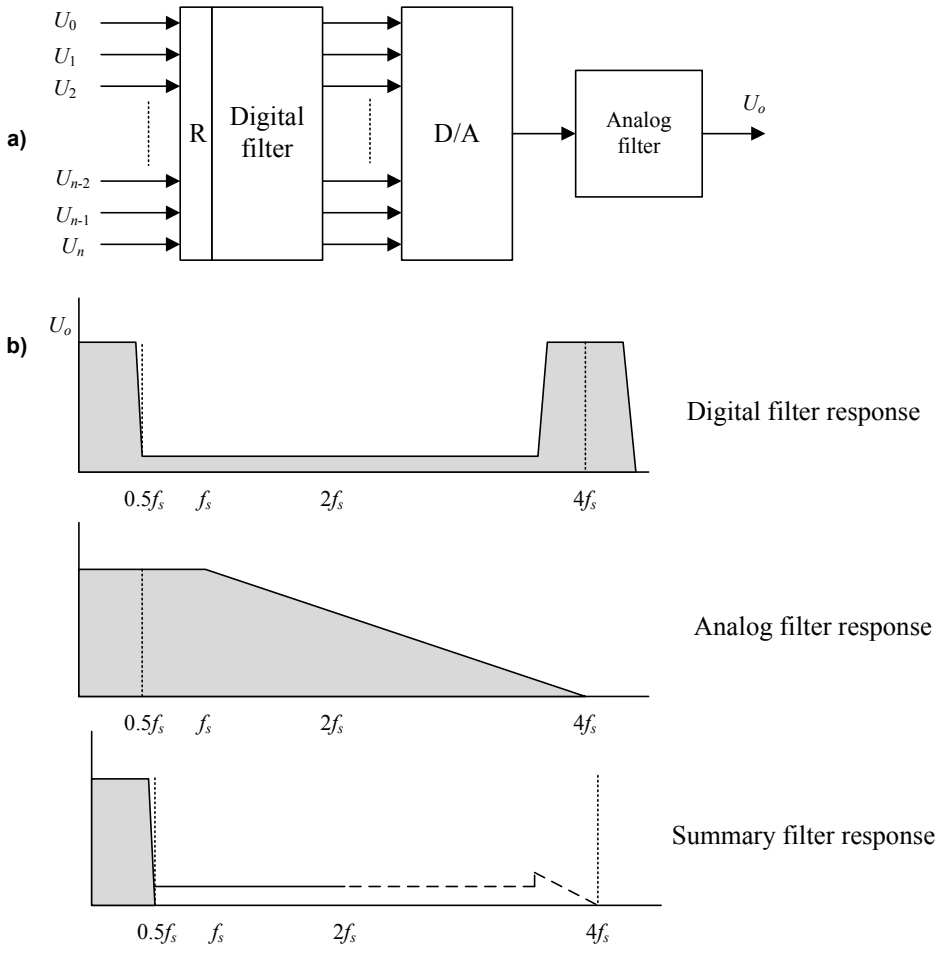


Fig. 6.5. D/A processing with analog and digital filtration
a) a scheme, b) the characteristics

6.2. A/D CONVERTERS

A/D converters processing analog signals to digital signals. It is a circuit with one input and n outputs. The result of conversion is a digital code proportional to analog output signal value. The A/D converter is performing the operation

$$U_I = U_{REF}\left(\frac{a_1}{2^1}+\frac{a_2}{2^2}+...+\frac{a_n}{2^N}\right). \tag{6.2}$$

A/D converter basis scheme is presented in Fig. 6.6. In the general case the A/D converter consist of one analog input and *N*-bit digital outputs. The analog input can change from –FS (FullScale) to +FS. The digital output gives information about input signal, with number of bits accuracy. The highest value of digital value

is given by the most significant bit MSB, the lowest value is given by the last bit LSB (less significance bit). If in the input analog signal, noises with high value are present, the A/D converter will not use all bits in the measurement process.

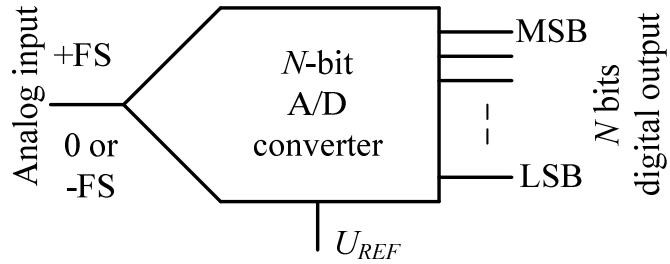


Fig. 6.6. Definition of A/D converter input and output

To use correctly any A/D converter, especially in renewable energy sources measurement systems, user must have a knowledge about converter parameters. To the basic parameters of A/D converters there can be enumerated:

1. *Conversion time* – is the time required for a complete measurement by an analog-to-digital converter.
2. *Resolution* - is the smallest analog increment corresponding to a 1 LSB converter code change. Resolution is normally expressed in bits, where the number of digital codes is equal to 2^N. As an example, a 10-bit converter maps the analog signal into $2^{10} = 1024$ digital codes.

$$\Delta U = \frac{U_{REF}}{2^N} \tag{6.2}$$

3. *Quantization error* - is the error inherent in all A/D conversions. Since even an 'ideal' converter has finite resolution, any analog voltage that falls beween two adjacent output codes will result in an output code that is inaccurate by up to 1/2 LSB.

$$q = \pm\frac{\Delta U}{2} \quad \text{or} \quad q = \pm\frac{LSB}{2} \tag{6.3}$$

   Fig. 6.7 presents the A/D converters transient characteristic with graphical representation of quantization error.
4. Integral non-linearity (INL) - is a measure of the deviation of each individual code from a line drawn from zero scale or negative full scale through positive full scale The deviation of any given code from this straight line is measured from the center of that code value. The graphical representation of DNL is presented in Fig. 6.27.

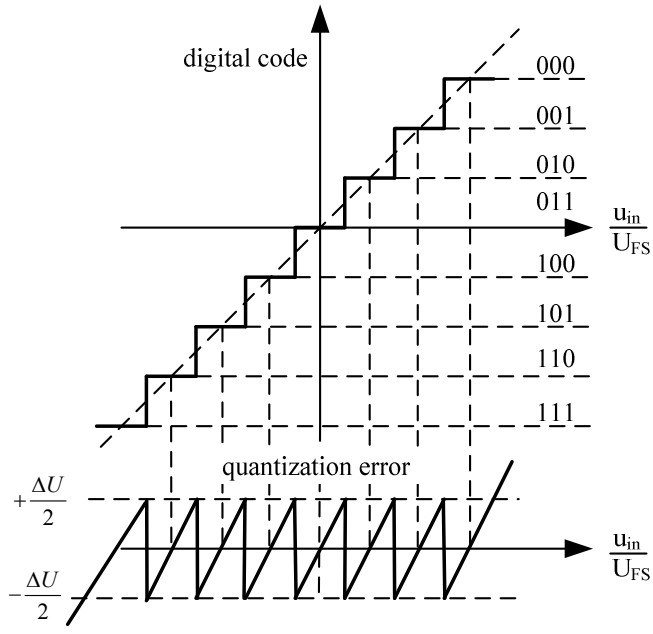


Fig. 6.7. The A/D transient characteristic [7]

5. Differential non-linearity (DNL) - is the measure of the maximum deviation from the ideal step size of 1 LSB. The graphical representation of DNL is presented in fig. 6.26.
6. Aperture delay - is the time after the edge of the clock to when the input signal is acquired
7. Analog input bandwidth - is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

A/D converters can be divided into three main groups depending on used processing method: compensation, integration and a new group sigma-delta. In this book there will be discussed only chosen converters, such as flash (parallel), serial with equably compensation, integrating and sigma-delta. All of this converters can be used in measurement systems to determine parameters of renewable energy sources.

6.2.1. Flash converter

The flash A/D converters are the fastest type of A/D converter and use large number of comparators. An *N*-bit flash A/D converter consists of 2^N resistors and 2^{N-1} comparators and is presented in Fig.6.8. Each comparator has a reference voltage from the resistor string which is 1 LSB higher than that of the one below it in the chain. For a given input voltage, all the comparators below a certain point

will have their input voltage larger than their reference voltage and a "1" logic output, and all the comparators above that point will have a reference voltage higher than the input voltage and a "0" logic output. The 2^{N-1} comparator outputs therefore behave in a way analog to a mercury thermometer, and the output code at this point is sometimes called a "thermometer" code. Since 2^{N-1} data outputs are not really practical, they are processed by a decoder to generate an *N*-bit binary output.

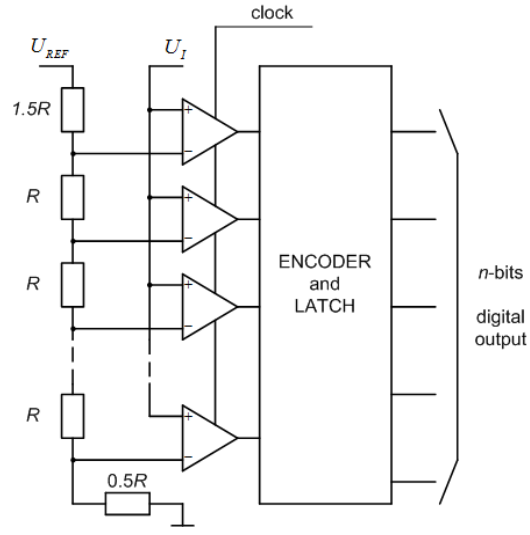


Fig. 6.8. *N*-bit flash converter

The input signal is applied to all comparators at the same time, so the digital output is delayed only by one comparator delay from the input and a few digital structures in encoder. This type of converter theoretically does not need sample-hold circuits because each of the comparators provide sample-hold function. To enhance the dynamic performance of flash converters usually there are used the external sample-hold circuits. The large number of reference voltages (resistors) and comparators results in limitation to build this type of converters with low resolutions (typically 10-bits) [16]. Because used comparators must be very fast so they are built in large chip sizes and their power consumption and power dissipation is relatively high. For correctly processing by flash converters there must be added an high quality (high accuracy) external clock. The flash converter still maintains its position as the fastest possible A/D converter architecture for a given IC process. However, power and real estate considerations generally limit the resolution to 8 or 10 bits. Today Gallium Arsenide (AsGa) flash converters are available with sampling rates over 1 GHz, however power dissipation limit their popularity.

6.2.2. Serial with uniform rate compensation converters

Ramp run-up converter architecture is shown in Fig. 6.9. The input signal u_{in} is applied to comparator. The clock and D/A converter (DAC), which is driven by the counter output, is started at the beginning of the conversion cycle. The counter measures the time required for DAC output value to equal the analog input voltage (Fig. 6.9). The counter output is proportional to the value of analog input.

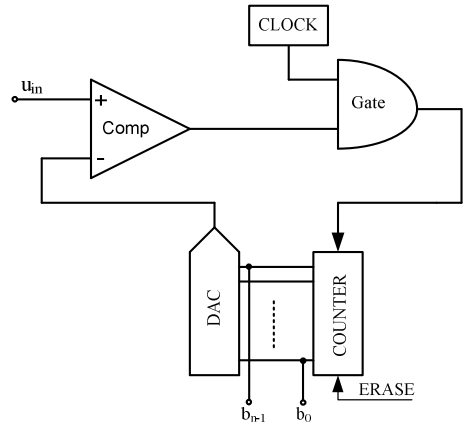


Fig. 6.9. A ramp run-up converter

The advantage of using this type of A/D converter is a monotonicity, which is determined by the D/A converter parameters.

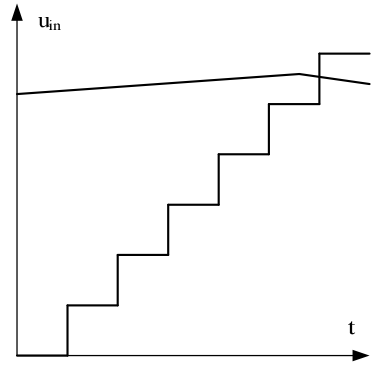


Fig. 6.10. Output signals of a rump run-up converter

The accuracy of the ramp run-up A/D converter depends on accuracy of the D/A converter and oscillator. When it is necessary to use this converter for AC signals (low frequency), a sample-hold circuit has to be used.

For low frequencies signals it is better to use the tracking A/D converter architecture, which is presented in Fig. 6.11. This type of A/D converter continually compares the analog input signal with reconstructed input signal from DAC output. The reverse (up-down) counter is controlled by the comparator output. If the D/A converter output exceeds the analog input, the counter counts down until they are equal. If the input signal exceeds the D/A converter output, the counter counts up until they are equal. If the input signal changes slowly, the counter follows (Fig.6.12).

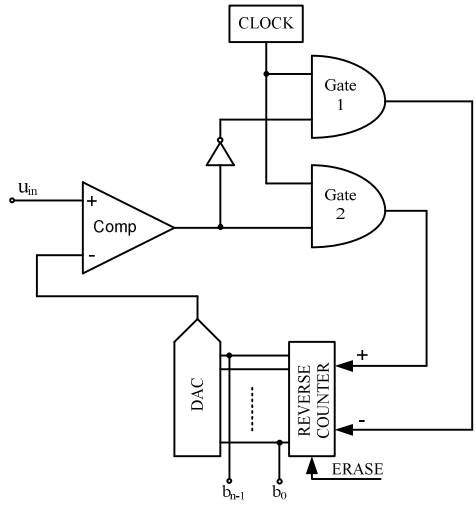


Fig. 6.11. A tracking A/D converter

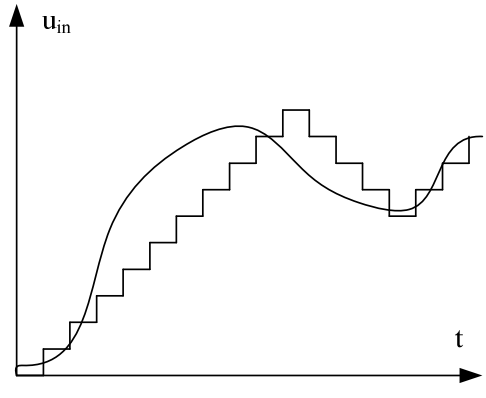


Fig. 6.12. Output signals of a tracking converter

The digital output then will be close to its correct value. If the input signal changes too fast, with high dynamic, then on the converter output there will a

wrong value occur. This converters can be used to measure the accumulators battery sources.

6.2.3. A dual slope integrating A/D converter

Introduced in the 1950s, the *dual-slope* A/D converter architecture was truly a breakthrough in A/D converters for high resolution applications such as digital voltmeters. A simple scheme is shown in Fig. 6.13.

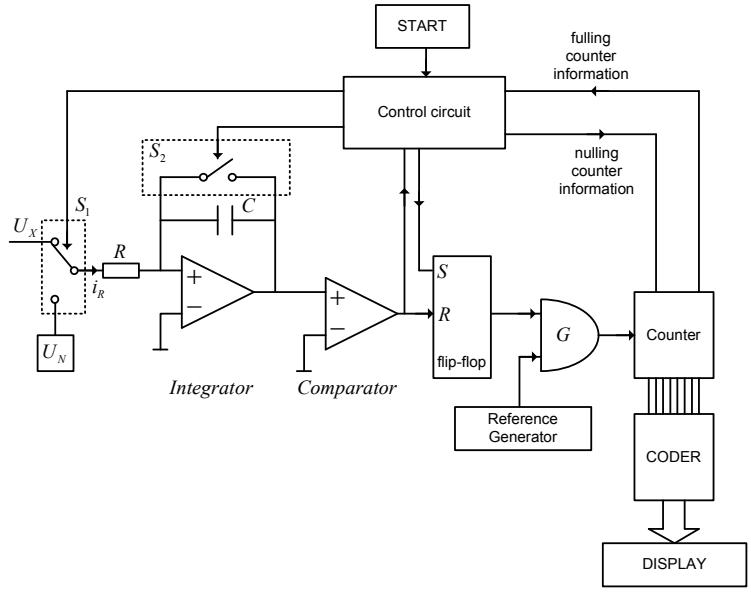


Fig. 6.13. A scheme of a dual slope integrating A/D converter

The input analog signal U_X is applied to an integrator. At the same time the counter is started and clock pulses from the gate output are counting. The measurement process consist of two parts:

1. the capacitor is charged by the current

$$i_R = i_C = \frac{U_X}{R}, \tag{6.4}$$

which is proportional to the input voltage U_X. At the time t_1, as it shown in Fig. 6.14, an integrator output voltage is described by

$$u_C(t_1) = \frac{1}{C}\int_0^{t_1} i_C dt = \frac{U_X}{CR} t_1 . \tag{6.5}$$

2. the capacitor is discharged by the current

$$i_R = i_C = -\frac{U_N}{R}, \tag{6.6}$$

because applied to the integrator input a reference voltage has opposite polarity. When the integrator output reaches zero, the count is stopped and the flip-flop is reset. At the time t_x an integrator output voltage is described by

$$u_C(t_X) = \frac{1}{C}\int_0^{t_X} i_C dt = \frac{-U_N}{CR} t_X . \tag{6.7}$$

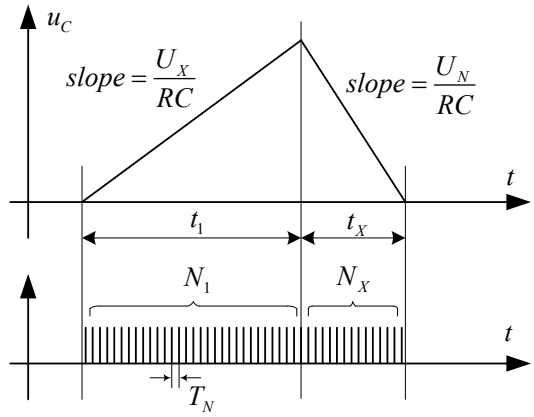


Fig. 6.14. The integrator output voltage and the counter characteristics

Because the charge gained is proportional to $U_1 t_1$ and the charge lost is proportional to $U_N t_X$ it can be written as relation to full scale integrating operation

$$u_C(t_1 + t_X) = u_C(t_1) + u_C(t_X) = \frac{U_X}{CR} t_X - \frac{U_N}{CR} t_X = 0 . \tag{6.7}$$

From relation (6.7) there was calculated the value of the input voltage

$$U_X = U_N \frac{t_X}{t_1} = U_N \frac{T_N N_X}{T_N N_1} = U_N \frac{N_X}{N_1} \tag{6.8}$$

Measured voltage is proportional to counted pulses ratio and reference voltage U_N.

Dual-slope integration has many advantages. The conversion accuracy is independent of both the capacitance and the clock frequency, because they affect both the up-slope and the down-slope by the same ratio. The fixed input signal integration period results in rejection of noise frequencies on the analog input that have periods which are equal or a sub-multiple of the integration time *T*.

Errors caused by bias currents and the offset voltages of the integrating amplifier and the comparator, as well as gain errors, can be cancelled by using

additional charge/discharge cycles to measure "zero" and "full-scale" and using the results to digitally correct the initial measurement.

6.2.4. Sigma – delta converter

The sigma-delta A/D converter is the converter of choice for high resolution (20, 24bits) precision research and industrial measurement applications.

Input analog signal in delta modulation is quantized by a one-bit A/D converter (in practical solutions it is usually a comparator with proper parameters). The delta modulation general circuit is presented in Fig. 6.15.

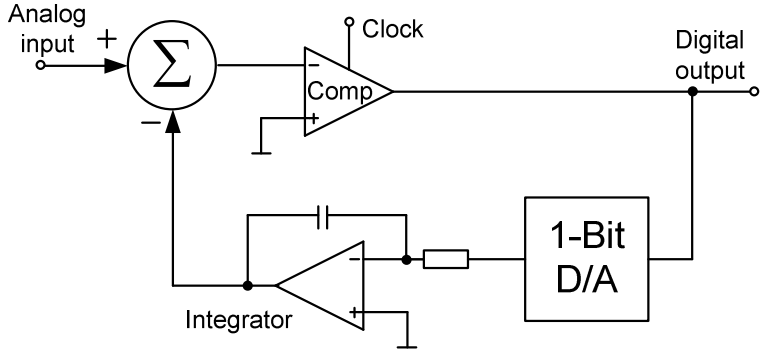


Fig. 6.15. Delta modulation

From the analog input there is a subtraction made with the output signal from the integrator. The output of the integrator (digital signal) is converted back into analog form by the 1-bit D/A converter. Then the signal is processed in the integrating circuit. The shape of the input signal is transmitted as follows:

- 1 – a positive excursion has occurred since the last sample,
- 0 – a negative excursion has occurred since the last sample.

The theoretical amplitude limitation of delta modulation is that the analog input signal cannot change too dynamically [16].

In differential PCM modulation the comparator was replaced by N-bit A/D converter to derive the processed information about signal parameters. This kind of modulation is shown in Fig. 6.16.

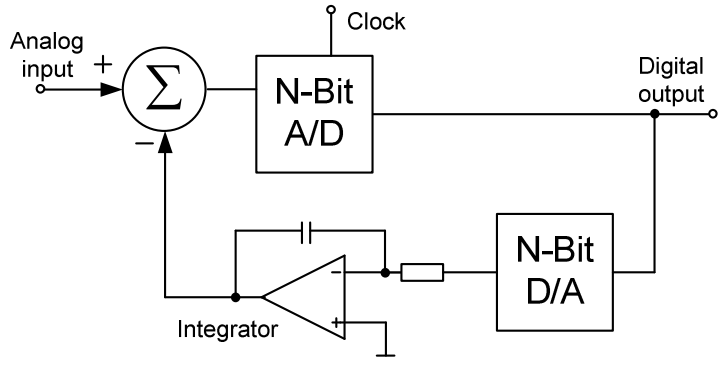


Fig. 6.16. Differential PCM modulation

A sigma-delta A/D converter contains simple electronic elements such as: comparator, voltage reference, switch, integrator and an analog summing circuits, together with a complex digital computational circuitry. The computational circuitry consist of a digital signal processor, which acts as a usually low pass filter [16].

To understand how the sigma-delta converter works, some additional parameters must be known, such as oversampling, quantization noise shaping, digital filtering and decimation. Technique of oversampling can be shown with an analysis in the frequency domain. Where DC conversion has a quantization error ½ LSB, a sampled data system has the quantization noise. As it is shown in Fig. 6.7 the equation for quantization error is given by

$$e(t) = st, -q/2s < t < +q/2s\,, \tag{6.9}$$

where s is a slope of the sawtooth waveform.

The mean-square value can be written as

$$\overline{e^2(t)} = \frac{s}{q}\int_{-\frac{q}{2s}}^{+\frac{q}{2s}} (st)^2\, dt = \frac{q^2}{12}. \tag{6.10}$$

An ideal classical N-bit sampling A/D converters has an RMS quantization noise $\sqrt{\overline{e^2(t)}}$ of $q/\sqrt{12}$ (q - value of a LSB) distributed within the Nyquist band from DC to $f_s/2$ (f_s - the sampling rate) as it is shown in Fig. 6.17a [7].

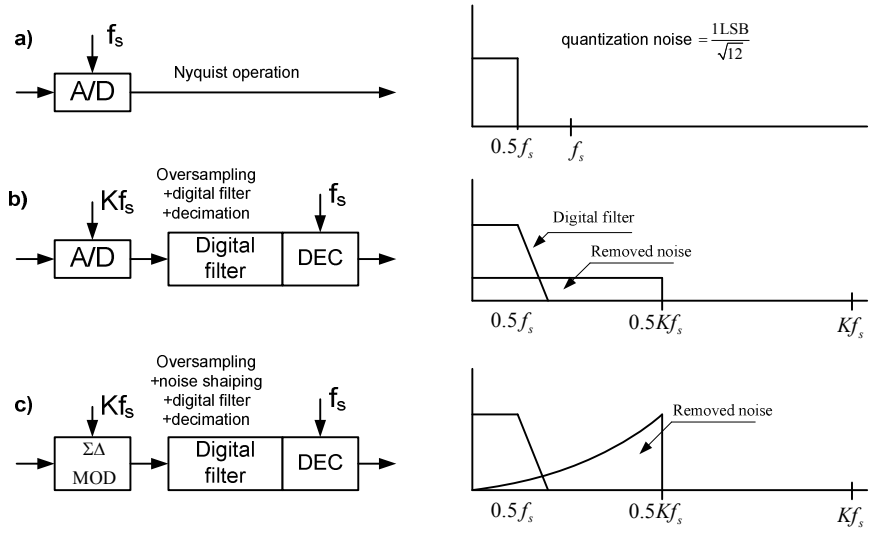


Fig. 6.17. Oversampling, digital filtering, noise shaping, decimation

The signal-to-noise ratio (SNR) can be calculated assuming that the input is a sine wave.

$$u_{\sin}(t) = \frac{q2^N}{2}\sin(2\pi ft). \tag{6.11}$$

The RMS value is

$$U_{\sin} = \frac{q2^N}{2\sqrt{2}}. \tag{6.12}$$

For ideal N-bit converter the RMS signal-to-noise ratio is therefore

$$SNR = 20\log\frac{U\sin}{\sqrt{\overline{e^2(t)}}} \tag{6.13}$$

$$SNR = 20\log\left[\frac{\frac{q2^N}{2\sqrt{2}}}{\frac{q}{\sqrt{12}}}\right] = 20\log 2^N + 20\log\sqrt{\frac{3}{2}} = 6.02N + 1.76\ \text{dB}$$

Therefore, its SNR with a full-scale sine wave input will be (6.02N + 1.76) dB [7, 34]. If the A/D converter is not ideal and its noise is greater than its theoretical minimum quantization noise, then its effective resolution will be less than *N*-bits. The real resolution is defined by

$$\Delta r_{ef} = \frac{SNR - 1.76\ \text{dB}}{6.02\ \text{dB}}. \tag{6.14}$$

Fig. 6.17b presents higher sampling rate with the multiplier Kf_s. In this case the noise is distributed over the bandwidth DC to $Kf_s/2$. To remove much of the quantization noise the digital low-pass filter must be added to the output. The wanted signal will be not affected. The factor K is referred as the oversampling ratio. Oversampling has an additional advantage – the requirements for the analog antialiasing filter are lower. It is a very important information for designers of measurement systems, where a sharp cut off linear phase filter can be significant.

Since the bandwidth is reduced by the digital output filter, the output data rate may be lower than the original sampling rate (Kf_s) and still the Nyquist criterion will be kept. This may be achieved by passing every mathematical result to the output and discarding the remainder. The process is known as decimation by a M factor, which can have any integer value, provided that the output data rate is more than twice the signal bandwidth. The decimation does not cause any loss of information.

The sigma-delta converter does not need such a high oversampling ratio because it not only limits the signal passband, but also shapes the quantization noise so, that most of it falls outside this passband as shown in Fig 6.16c.

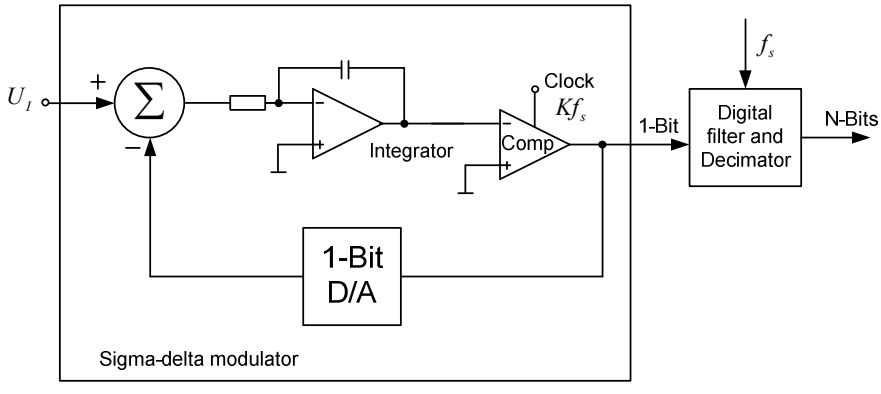


Fig. 6.18. A first order sigma-delta A/D converter

First order sigma-delta modulator is presented in Fig. 6.18. It consist of a comparator, an integrator, a 1-bit D/A converter, digital low pass filter and a decimator at the digital output. The sigma-delta modulator shapes the quantization noise so that it lies above the passband of the digital output filter and the Δr_{eff} is larger than would be expected from the oversampling ratio.

The sigma-delta A/D converter operates as following.
Assume a DC input at U_I. The integrator is constantly ramping up or down at the output. The output of the comparator is fed back through a 1-bit D/A converter to

the summing input at inverted input of adder. The negative feedback loop, from the comparator output, through the 1-bit D/A converter, back to the summing point, will force the average DC voltage at the D/A converter output to be equal to *UI*. This implies that the average D/A converter output voltage must equal the input voltage *UI*. The average D/A converter output voltage is controlled by the 1-bit data stream from the comparator output.

Modern multimeters, as Agilent 34405A, has implemented the sigma-delta A/D converters on board. The general scheme of sigma-delta modulator used in instrumentation is presented in Fig. 6.19.

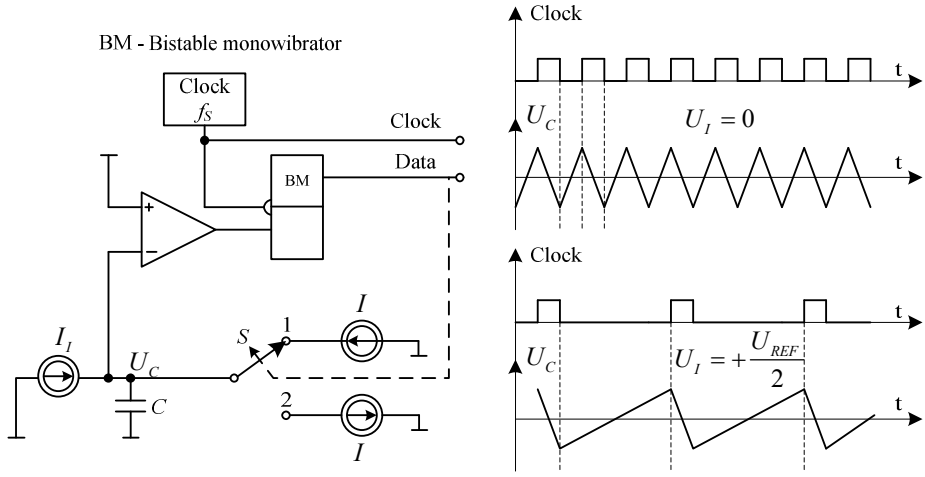


Fig. 6.19. Sigma-delta modulator [16]

The input signal is applied to the converter as the current I_I. The charge and discharge reference currents are noted by *I*. The signal is integrated by the capacitor *C*. The voltage on the capacitor is monitored by the comparator, which drives the bistable monovibrator BM. The BM is toggled by a system clock f_s. The output of the BM controls the switch *S* that switches the charge and discharcge currents to the capacitor *C*. When the input signal is equal zero, then a triangular wave is generated on the capacitor *C* as shown on Fig.6.18b. The average voltage value on the capacitor is zero. When an input signal is applied, then the one-zero pattern changes. The output of the BM, called Data, to an up-down counter performs the conversion of the 1-bit sigma-delta signal into a binary weighted output signal. The Fig. 6.20 shows the total digital voltmeter system.

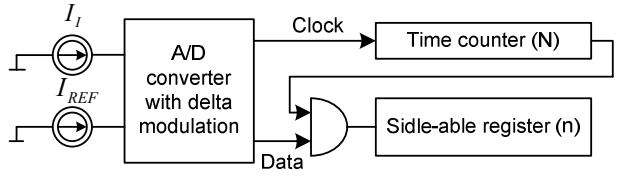


Fig. 6.20. A digital voltmeter system

To A/D sigma-delta converter a time counter, up-down counter (sidle-able register) and a gate are added. The timer function counts the total amount of up and down pulses. During this time the gate is opened and the difference between up and down pulses is counted by sidle-able register. Then the gate is closed and the system must be reset to start the next conversion cycle.

The ratio between the analog input signal and the reference current is described by the relation

$$\frac{I_I}{I_{REF}} = \frac{n_{forward} - n_{backward}}{n_{forward} + n_{backward}} = \frac{n}{N}. \tag{6.15}$$

The conversion time is determined by the frequency clock f_s

$$T_S = \frac{N}{f_S}. \tag{6.16}$$

When the conversion time T_S is related to the power line frequency, then due to the integration of a period of the power line frequency, a very good rejection of this frequency is obtained.

6.3. D/A CONVERTERS

The D/A converter is processing a digital signal into a analog signal. It is a circuit with n inputs and one output. The result of conversion is a analog signal proportional to digital input code.

General equation of voltage D/A converter:

$$U_o = U_{REF} N \tag{6.17}$$

Typical D/A converter architecture is shown in Fig. 6.21.

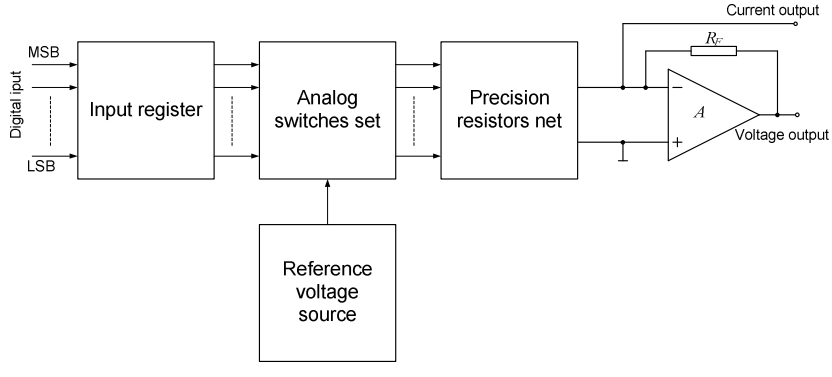


Fig. 6.21. A general D/A converter architecture

Classification of D/A converters

It are a few possibilities of D/A converters classifications, which result from:

- kind of precision resistor net used (binary-weighted resistor, *R*-2*R* ladder network),
- kind of reference signal source – converters with internal and external reference source,
- kind of mark output quantity – unipolar and bipolar converters,
- kind of output quantity – voltage or current.

6.3.1. Binary-weighted D/A converter

The voltage-mode binary-weighted resistor D/A converter is shown in Fig. 6.22. This D/A converter is not inherently monotonic and is quite hard to produce at high resolutions. The output impedance of the voltage-mode binary D/A converter changes with the input code.

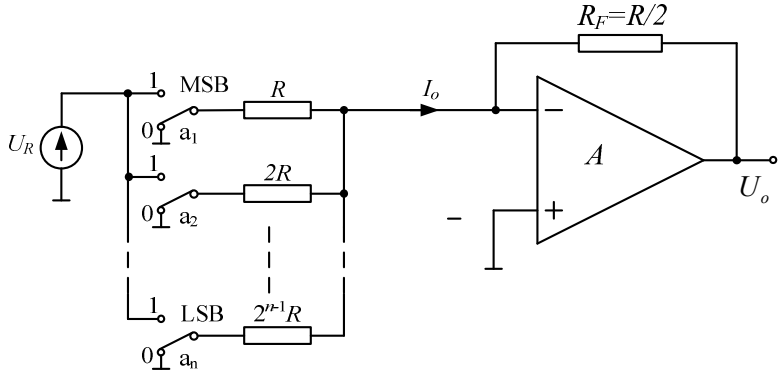


Fig. 6.22. A voltage-mode binary-weighted D/A converter

If the MSB current is low in value, it will be less than the sum of all the other bit currents, and the D/A converter will not be monotonic. This architecture is used version as components in more complex circuits (max 4-bit converters).

6.2.1. R-2R D/A converter

One of the most common D/A converter structures is the R-2R resistor ladder network presented in Fig. 6.23. This architecture was proposed by B. D. Smith in 1953. It uses high precision resistors of only two different values, with ratio 2:1. An *N*-bit D/A converter requires 2^N resistors and they are easily trimmed. Switching between reference voltage source and ground and the output is taken from the end of the ladder. The output may be taken as a voltage, but the output

impedance is independent of code, so it may equally well be taken as a current into a virtual ground.

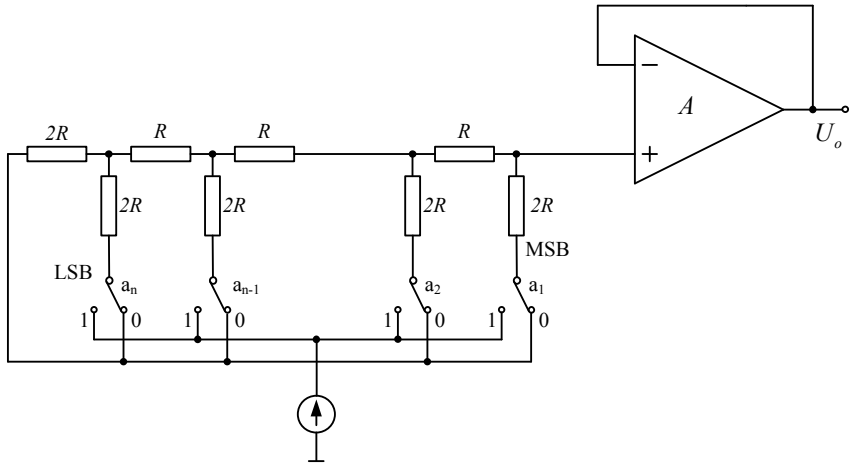


Fig. 6.23. Voltage-mode R-2R D/A converter

6.4. COMPARISON OF ERRORS OF A/D AND D/A CONVERTERS

Four basic A/D and D/A converters processing errors could be shown. It is decided by processing accuracy of converters. For this errors can be count:

1. Zero error defined as a difference between the nominal and actual zero point position. The graphical representation is shown in Fig. 6.24.

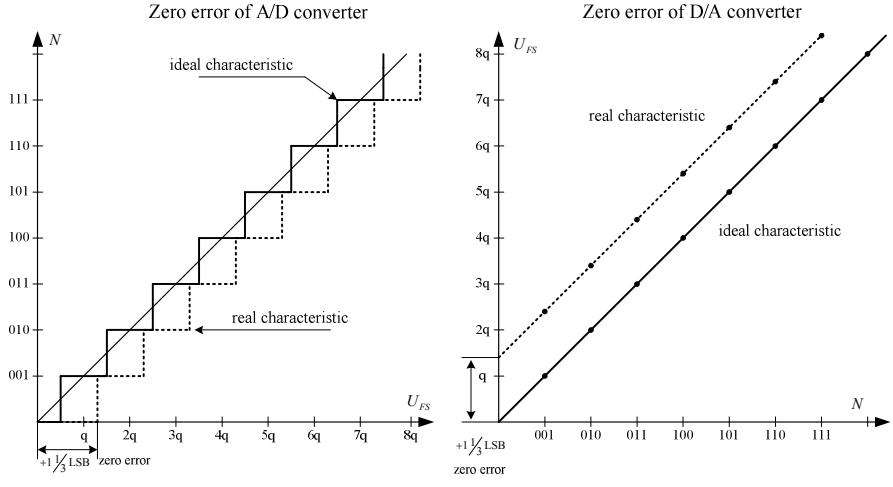


Fig. 6.24. The zero error of A/D and D/A converters

2. Gain error is defined after zero error compensation process. In case of the A/D converter it is a difference between the nominal, maximum value of input signal and the median value in the last step of quantizing process. The gain error for D/A converter is determined as difference between the nominal and actual measured points position, which came up to full-scale processing. The gain error is presented graphically in Fig. 6.25.

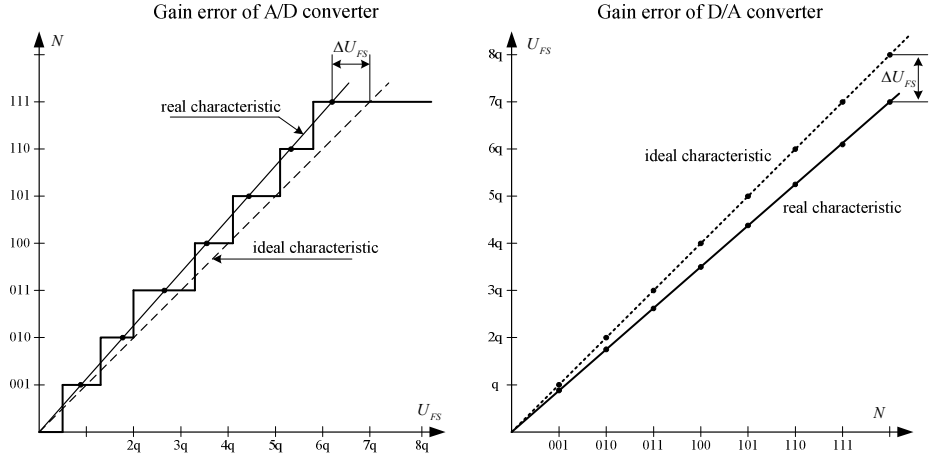


Fig. 6.25. The gain error of A/D and D/A converters

3. Differential non-linearity error is defined as the difference between current width of quantizing step (in the case of A/D converter) or the height of quantizing step (for D/A converter) and the LSB step theoretical value. The graphical representation is shown in Fig. 6.26.

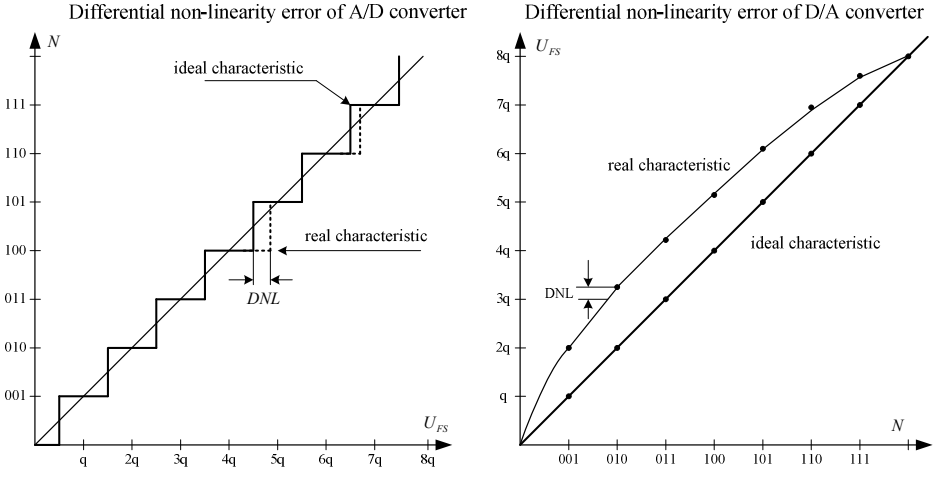


Fig. 6.26. The differential non-linearity error of A/D and D/A converters

4. Integral non-linearity error is the values deflection of measured processing characteristic from the straight line connected with ideal processing. Several methods are possible to reference lines determination. In the basic solution the reference line connects zero point with full-scale point. It can be done after the zero and gain error compensation process. For the A/D converter errors should be measured in every quantizing step. The graphical representation is presented in Fig. 6.27.

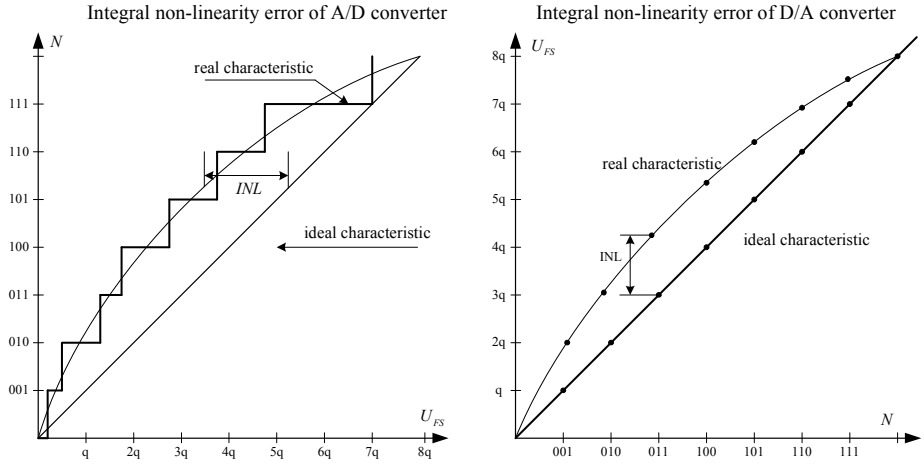


Fig. 6.27. The integral non-linearity error of A/D and D/A converters

7. MEASUREMENT DISTURBANCES ATTENUATION

7.1. INTRODUCTION

Measurement instruments working conditions can be divided into:

- static conditions,
- dynamic conditions.

The measurement errors can be divided in the similar way.

Digital instruments are characterized by a few profitable properties:

- the parallax error does not exist – high measurand reading comfort,
- high measurement process speed,
- usually high accuracy,
- measurement process automation possibility – instruments with standard interfaces.

Digital instrument accuracy is defined by relation

$$\pm\left(a\%\ \text{reading} + b\ \text{digits}\right), \tag{7.1}$$

where *b* digits stands for the multiplying of the b value and resolution of used digital instrument.

Digital instruments resolution is defined as the last digit of a reading. For multirange instruments the resolution depends on measurement range. For example:

- Range is $U_n = 100\ \text{V}$, the reading is $U = 94.56\ \text{V}$ - resolution for this result is $\Delta_r U = 0.01\ \text{V}$,
- Range is $U_n = 100\ \text{mV}$, the reading is $U = 34.18\ \text{mV}$ - resolution for this result is $\Delta_r U = 0.01\ \text{mV}$.

Example 1.
Instrument accuracy is defined by equation: $0.5\%U_x + 2$ digits. The instrument range is 2.000 V; measurement reading is $U_x = 1.658$ V. Calculate the limiting errors.

For this measurement the resolution was $\Delta_r U = 0.001\ \text{V}$, so

$$\Delta_l U = \frac{0.5\ \%\ 1.658\ \text{V}}{100\ \%} + 2 \cdot 0.001\ \text{V} = 0.0083 + 0.002 = 0.0103\ \text{V} = 0.010\ \text{V}$$

$$\delta_l U = \frac{0.0103\ \text{V}}{1.658\ \text{V}} \cdot 100\ \% = 0.62\ \%.$$

Some instruments have described accuracy by other equation

$$\pm\left(a\%\ \text{reading} + c\%\ \text{full scale range}\right). \tag{7.2}$$

As it is shown in relation (7.1) and (7.2) the integral error consist of two components. The first component - a% reading, stands for the relative analog error component. Analog error is a sum of a few components:

- instrument sensitivity error threshold,
- reference quantity source error,
- noises.

The second component stands for the digital error component, which can be defined as a relative or absolute value.

If the reading is near full scale range then the analog component is dominant in limiting error value. In the other way (low values measure) the digital component is dominant.

Example 2.

Instrument accuracy is given as: $0.5\%U_x + 0.1\%U_R$.

The reading value was 102.3mV. The instrument range was 200mV.

The limiting absolute and relative errors

$$\Delta_l U = \frac{0.5\,\%\,102.3\text{ mV}}{100\ \%} + \frac{0.1\,\%\,200\text{ mV}}{100\,\%} = 0.5115 + 0.2 = 0.71\text{ mV}$$

$$\delta_l U = 0.5\,\% + 0.1\,\%\frac{200\text{ mV}}{102.3\text{ mV}} = 0.5\,\% + 0.196\,\% = 0.70\,\%.$$

In instrumentation the sources of dynamic errors can be numbered as:

- measured quantity change in time when the measurement is carried out,
- sampling,
- measurement instrument transient states

In Fig. 7.1 the averaging error in A/D conversion, as a result of integrating or sampling process, is presented.

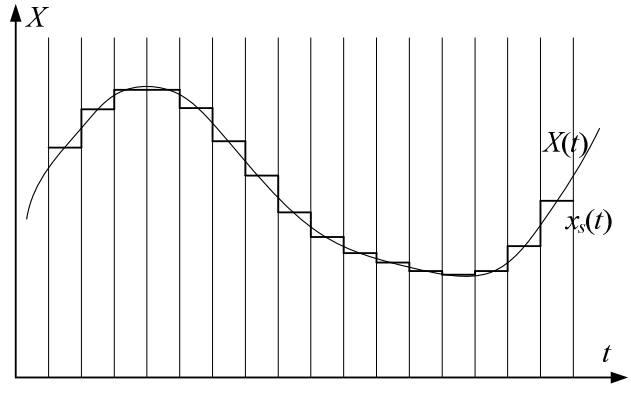


Fig. 7.1. The A/D conversion averaging error

Modern high resolution and high speed instruments give the choice of two configurations for high speed measurements: a 100 kHz bandwidth integrating path or a 10 MHz bandwidth path with 16-bit of resolution sample-hold circuit. The configuration of measurement path is shown in Fig.7.2.

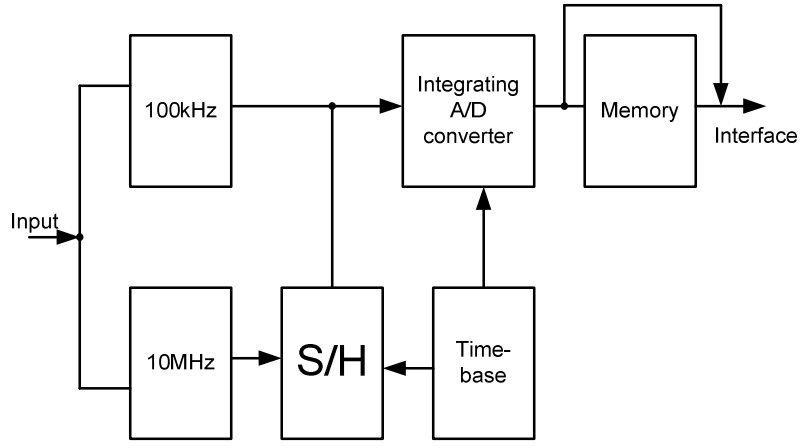


Fig. 7.2. Digitizing configurations

The integration path is used to lower the noise and the sample-hold path is used to precisely capture the voltage at a single point on a waveform. It is especially important in sensor and converters tests, when signals must be taken from the specific point on a waveform.

7.2. TECHNIQUES OF DISTURBANCES ATTENUATION

There are many techniques for disturbances attenuation in a measurement system. Here it is achieved by proper shielding, wiring and termination.

Proper shielding gives certainty that some types of external noises will not influence the correct measurement results. The correct wiring and particularly termination is very important for the low level signal measurement. When disturbances, especially in the renewable energy sources has high values, then the best shielding is not sufficient. Then the best solution for reduction of measurement disturbances is adding a correctly designed electronic circuit, to ensure better disturbances immunity. This knowledge is very important in measurement systems with virtual instruments, which are using data acquisition cards. In high accuracy measurements it is needed to use high precise data acquisition (DAQ) cards. Sometimes the external or measurement method is followed by disturbances, causing that the real resolution of the DAQ card is much lower than it was designed for the measurement system. There are known a few techniques for achieving more accurate measurement results [36].

7.2.1. Rejecting of the DC common-mode voltage

The first technique is the DC common-mode voltage rejecting. To make highly accurate measurements it is useful to start with differential readings. An ideal differential amplifier, as it was shown in Chapter 1, reads only the potential difference between the positive and negative inputs. Real amplifiers are limited to reject common-mode voltage. In Fig. 7.3, when voltage sources E_1 and E_2 are equal 4.5V, then the potential on inverting input will be 4.5V and on the non-inverting input will be 9.0V.

$$U_o = E_1 - E_2 = 9.0\ \text{V} - 4.5\ \text{V} = 4.5\ \text{V}. \tag{7.3}$$

The ideal amplifier reads the resulting 4.5V difference between the two inputs.

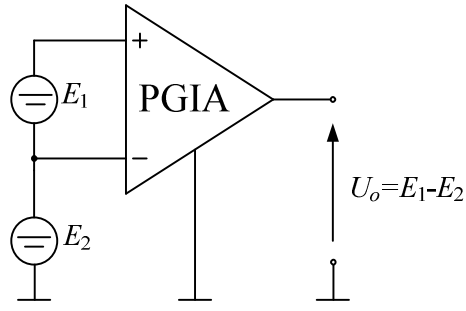


Fig. 7.3. An ideal amplifier.

The maximum voltage of a data acquisition card is the same as the input range of the instrumentation amplifier, located on the beginning of processing lane. Almost all PCI, PCIe DAQ card have the input voltage limited to 11 V, because instrumentation amplifiers are supplied by voltage ± 12 V . Higher, than 11 V input signals can cause damage to the amplifier. When the input signal has higher values, then it is necessary to build in a voltage divider. In some applications the voltage dividers (from resistors) cannot be used, because a circuit with galvanic isolation is needed. Then there can be used a voltage instrument transformer or a voltage inductive divider. This solution has a few disadvantages: the cost of measurement system can be much higher than it was assumed at the beginning and additional errors have to be calculated. Input signals can be up to 300 V RMS in channel-to-channel isolation type and to ± 60 V in channel-to-earth ground isolation type. Isolation can increase the input voltage of a DAQ card. Isolation here means physical and electrical separation of two parts of a circuit. An isolator amplifier *IsA* passes data from one part of the measurement lane to another without conducting electricity, so the current cannot flow across isolation barrier. You can level-shift the DAQ device ground reference away from earth ground. Usage of the isolation amplifier, to isolate instrumentation amplifier ground reference on DAQ card from earth ground, is presented in Fig. 7.4 [36].

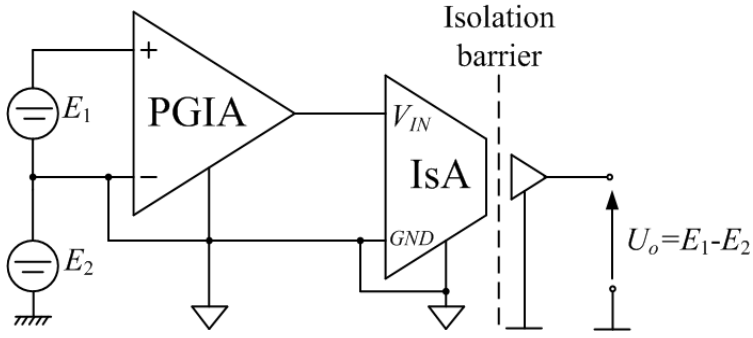


Fig. 7.4. Use of the isolation amplifier in systems with DAQ cards

While the difference between the inverting and non-inverting input signals will be the same as that in (7.3), the E_2 source voltage can be extended to +60V, rejecting 55.5 V of common-mode voltage.

$$U_o = E_1 - E_2 = 60\ \text{V} - 55.5\ \text{V} = 4.5\ \text{V}\,. \tag{7.4}$$

The maximum voltage is defined by the isolation amplifier input parameters.
As an example application there can be given the accumulator battery testing, which are often used to accumulate current from photovoltaic panels. This application needs high DC CMVR. Each individual accumulator has a voltage equal exactly to 6 V, but the accumulator battery has a voltage value equal 6 kV. To measure the voltage of a single 6 V accumulator with high accuracy, with usage of a DAQ card, it is necessary to design the proper additional circuit consisting of isolation amplifiers, to reject the high common-mode voltages generated by the rest of the accumulator battery.

7.2.2. AC common-mode voltage rejecting

Most renewable energy sources of common-mode voltage contain an AC component. The measured signal disturbance is coupled with the nearest electromagnetic environment. This type of disturbance is especially important for low-level analog input signals lead to the input of DAQ cards.

Sources of AC disturbances can be classified by their coupling mechanisms [36]:

- radiation coupling – results from the electromagnetic field source when it is far from the measurement system (fluorescent lighting, electric and magnetic field)
- capacitive coupling - results from time-varying electric fields, when they are near (relays, other measurement signals, power lines).
- inductive coupling - results from time-varying magnetic fields (drives, machines, inductive converters).

In those cases, the AC common-mode voltage is coupled onto the measured signal, very often with power-line frequency. An ideal instrumentation amplifier, as the input circuit of DAQ card, can completely reject any AC-coupled disturbance. A real instrumentation amplifier can reject common-mode voltage with a parameter described as common-mode rejection ratio (CMRR). The CMRR is the ratio of the measured signal gain to the common-mode gain. It is describing by following equation:

$$CMRR_{IA} = \frac{A_u}{A_{us}}.$$

DAQ card with higher value of CMRR is characterized by better disturbance immunity. Characteristics in Fig. 7.5 show the difference between CMRR for a NI PCI 6224 DAQ card and much better NI PCI 6233 DAQ card manufactured by National Instruments company.

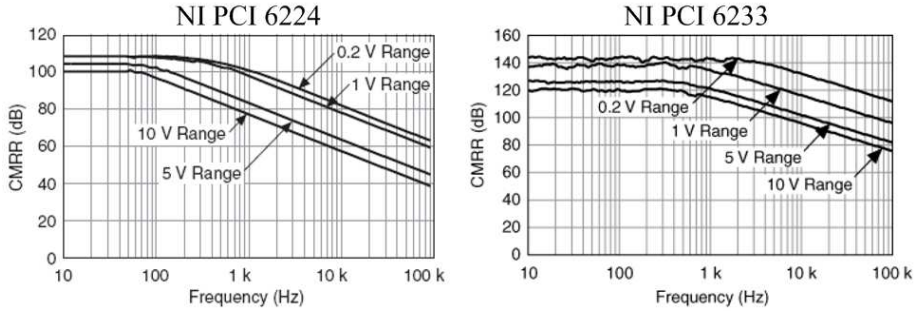


Fig. 7.5. CMRR comparison for NI PCI 6224 and NI PCI 6233 DAQ cards [36]

At 50 Hz, NI 6233 DAQ card has a 20 dB greater CMRR than NI 6224 DAQ card. This is equivalent to a 10 times better attenuation of 50 Hz (power-line frequency in Europe) disturbance. At 1 kHz, NI 6233 DAQ card reject noise 100 times better than NI 6224 DAQ card. This property is making DAQ cards with high CMRR value ideal for renewable energy applications.

7.2.3. Break ground loops

Ground loops are probably the most common source of disturbances in data acquisition systems. As one of the professors said: *The correct grounding is essential to properly working circuits and accurate measurements*. A ground loop forms when two connected terminals in a circuit are at different ground potentials. The difference is caused by current *i*, which flows between the signal source ground and the instrumentation amplifier ground. The current *i* in this situation, shown in Fig. 7.6, can produce offset errors [36].

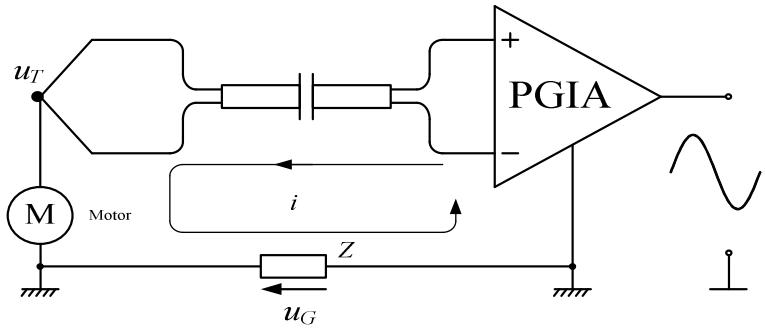


Fig. 7.6. A differential thermocouple wrong measurement.

The voltage potential between measured object ground and DAQ card ground includes DC and usually a power-line frequency additional signal. On the instrumentation amplifier output we have the result of interested signal and the disturbance.

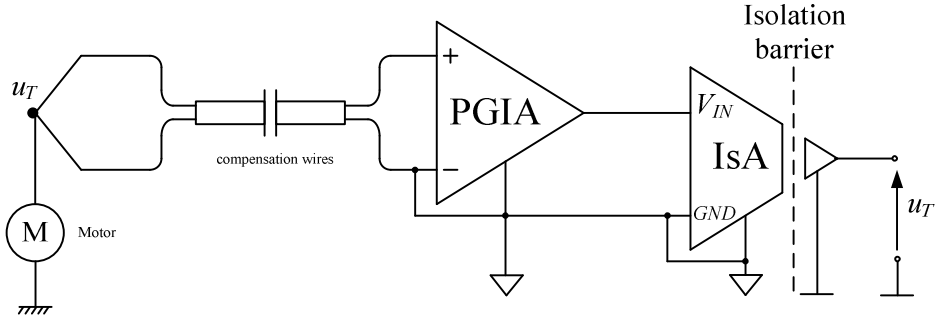


Fig. 7.7. Eliminating ground loops

This results in a signal that reveals power-line frequency components in the readings. The difference in ground potential could be even 200 mV or more if the power distribution circuits are not properly connected.
Because isolation is electrically separating, there can be added an isolation amplifier to isolate signal source ground from the instrumentation amplifier ground reference. This solution is presented in Fig.7.7.
Current *i* cannot flow across the isolation barrier and the amplifier ground reference can be at a higher or lower potential than earth ground.

7.2.4. 4-20 mA current loops

When the level of disturbances is very high, because of the distance to send the measurement information. Then is very difficult to design properly working accurate voltage measurement system and it is necessary to look for other solution.

Industrial converters that sense pressure, flow, proximity and so on, have a current output. A 4-20 mA current loop is a good method of sending sensor information over long distances in applications consisting of many kind of sensors. The example solution is shown in Fig.7.8.

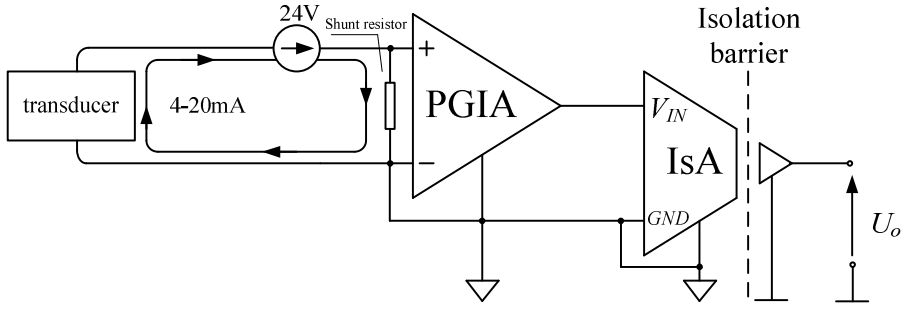


Fig. 7.8. A 4-20mA current loop circuit

Each of current loops contains three components – a sensor, a power source and a DAQ card. The current signal from the sensor is between 4 and 20 mA, where 4 mA represents the lowest signal value and 20 mA represents the maximum signal value. 0 mA value indicates an open circuit or bad connection and warning, that nothing can be done until the indication will be corrected. The current loop is usually supplied by 24 V or 30 V DC voltage source.

A high-precision shunt resistor between the inputs of the instrumentation amplifier is designed for convert the current signal into a voltage signal. Current loops are characterized by high immune to most sources of electrical disturbances and voltage drops.

7.2.5. 24 V digital logic

Measurement disturbances are not limited to analog signals. Digital logic may also be affected by a noisy electrical environment. It could be the case, when the digital gate indicates false “0’s” or “1’s” . For industrial applications, the logic standard TTL (0-5V) has the inherent disadvantage of small disturbance margins. With high logic level 2.0 V and low logic level 0.8 V there is a little margin for error (Fig. 7.9). When the disturbance has higher value than 0.3 V then the logic signal is shifted into an undefined region 0.8 V and 2.0 V and the output gate status is uncertain and may produce incorrect values. 24 V logic circuits offers increased disturbance immunity.

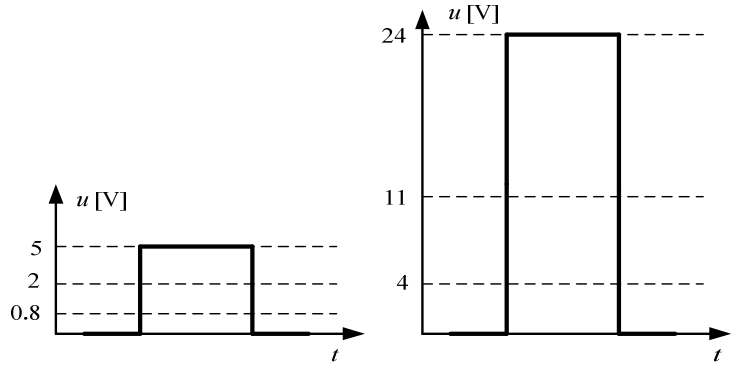


Fig. 7.9. Comparison of logic levels between the TTL standard and the industrial standard

A lot of industrial sensors, converters and actuators already operate at 24 V power supplies, so it is natural to use the 24 V digital logic level.

8. SENSORS AND TRANSDUCERS

Outputs of typical sensors are presented in table 8.1

Table 8.1 Typical sensors outputs

Property	Sensor	Active/Passive	Output
Temperature	Thermocouple	Passive	Voltage
	Silicon	Active	Voltage/Current
	RTD	Active	Resistance
	Thermistor	Active	Resistance
Force / Pressure	Strain Gage	Active	Resistance
	Piezoelectric	Passive	Voltage
Acceleration	Accelerometer	Active	Capacitance
Position	LVDT	Active	AC Voltage
Light intensity	Photodiode	Passive	Currrent

8.1 INDUCTIVE CURRENT TRANSDUCERS AND SENSORS

There are two methods for electric current processing to a measurement useful signal:

- voltage drop on reference resistor (doesn't ensure galvanic insulation)
- magnetic feedback of an output circuit with current circuit.

Measurement signal of industrial frequency current, adjusted to modern measurement circuits, should be generated in a galvanic insulation circuit from the current circuit.

The energy in the power system is carried by the current in the conductors, whose potentials differ significantly from the potential of zero. Current sensor network must provide galvanic insulation circuit signal from the circuit. Natural galvanic insulation is obtained by inductive coupling circuit.

To process the current network the current transformers (CTs) are commonly used. The current transformer circuits are coupled by a magnetic flux closure in the ferromagnetic magnetic core (Fig.8.1). Signal current (the secondary) in the circuit is roughly proportional to the current processed (the original). Error processing is caused by the current polarization, which is necessary to produce magnetic flux in a ferromagnetic magnetic core. Current polarization and therefore the processing error mainly depends on the permeability of the magnetic core and the parameters of the transformer. CT has a limited range of linearity, narrow bandwidth frequency and doesn't move the DC current.

The current transformer is processing the original current value i_1 on to proportional secondary current value i_2

$$i_2 = \frac{N_1}{N_2} i_1 = p\, i_1 . \tag{8.1}$$

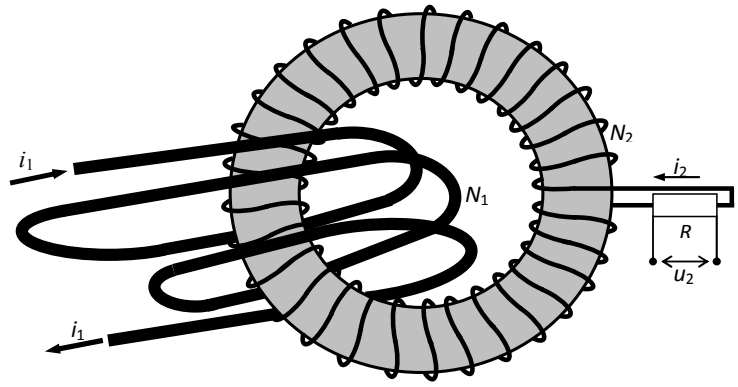


Fig. 8.1. A current transformer

The current i_1 processing error on to proportional current value

$$\Delta i_1 = i_1 - \frac{N_2}{N_1} i_2 = i_0 \tag{8.2}$$

and relative error

$$\delta i_1 = \frac{i_0}{i_1} . \tag{8.3}$$

Because

$$H_0 = \frac{i_0 N_1}{l_0} , \tag{8.4}$$

then

$$\delta i_1 = \frac{H_0 l_0}{i_1 N_1} . \tag{8.5}$$

In practical applications we assume that currents i_0, i_1, i i_2 are sinusoidal and CT errors are related to RMS values of this currents. There are two error components: module error (ratio error)

$$\delta I_1 = \frac{I_0'}{I_1} \tag{8.6}$$

and angle error – the angle between the I_1 and I_2 vector

$$\gamma = \frac{I_0''}{I_1}, \tag{8.7}$$

where I_0', I_0'' – are the components of polarization current: consistent and perpendicular to I_1 current vector.

Less values of errors are given by dual-core current transformers. The first solution with usage of two CTs was presented in 1922 by H.B. Brooks and F.C. Holtz. First current transformer processed the original current value to secondary circuit with 0.1% error, the second CT forced current in secondary circuit, which was proportional to magnetizing current i_0. If the second CT has a 10% error and the main CT has error 0.1%, then the Brooks-Holtz CT has error 0.01%. The scheme of Brooks-Holtz CT is shown in Fig. 8.2.

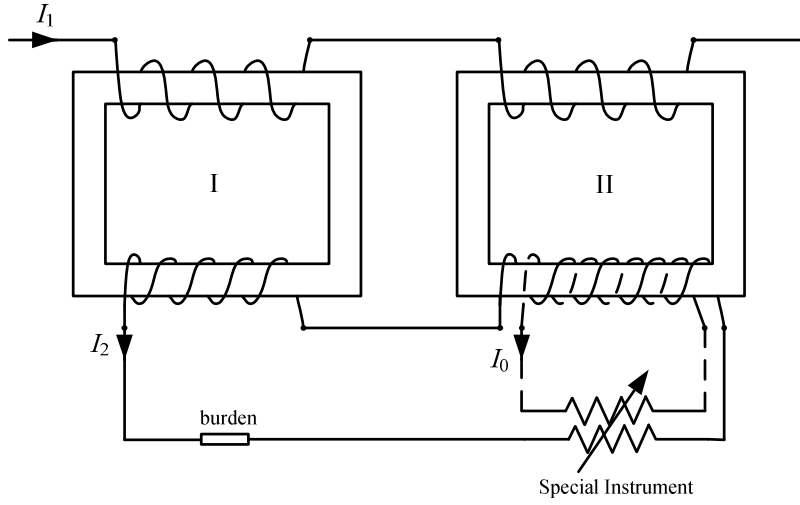


Fig. 8.2. Brooks-Holtz current transformer

CT I works as the main CT, however CT II has the additional, third winding, through which flows the current proportional to the magnetic current. Total value of secondary current is proportional to original current. This CT found the application as a standard CT in the CTs test system, which idea is presented in Fig. 8.3. In this system, worked out by Schering and Alberti, the compensation method is used. With the voltage drop on R_1 and R_2 resistors the voltage drop is compared on R_x resistor produced by secondary current of tested CT. The potentiometer and capacitor settings describes the errors of tested current transformer *X*.

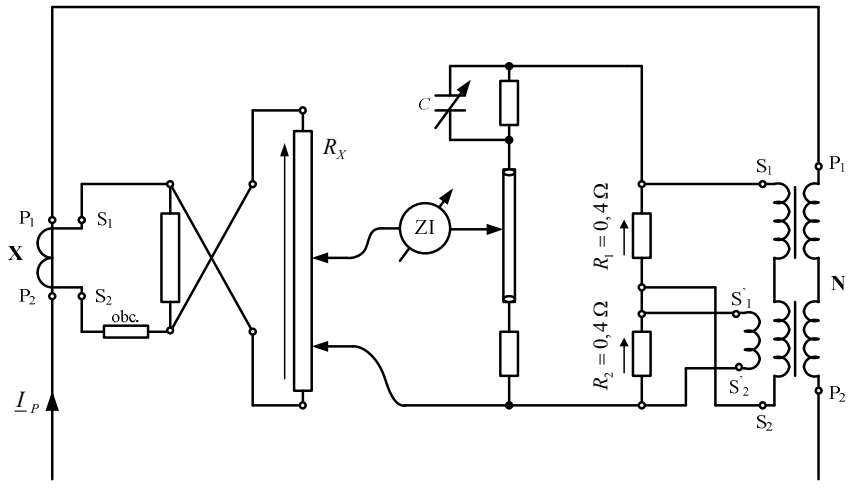


Fig. 8.3. Brooks-Holtz CT used in the CT test system

The CTs ,with ratio k_{In} = 1 A/A, metrological properties are determined in the test circuit with usage of a compensate-differential method. The Brooks-Holtz CT can be tested in the circuit shown in Fig. 8.4.

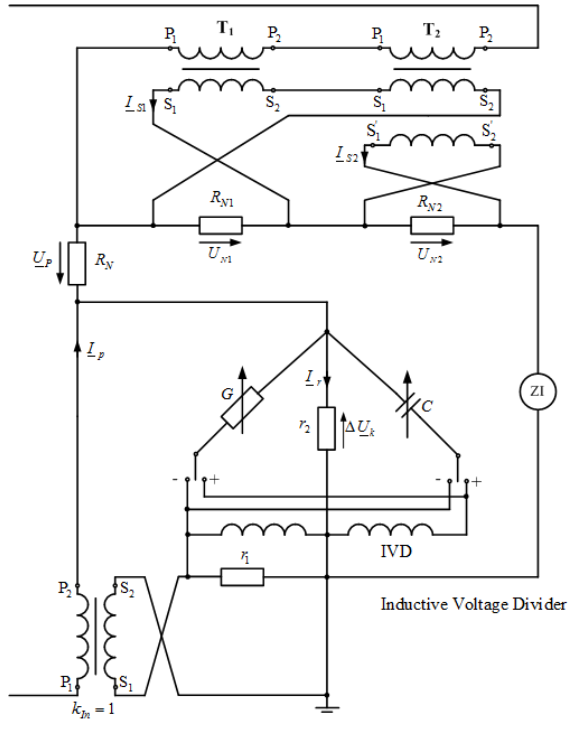


Fig. 8.4. Brooks-Holtz CT test system

In this circuit the currents: original and secondary, are comparing indirectly by the voltage drops on resistors R_N i R_{N1}, R_{N2}.

The tested CT error

$$\delta \underline{I} = \frac{\underline{I}_S k_{In} - \underline{I}_P}{\underline{I}_P} = \frac{\underline{I}_S - \underline{I}_P}{\underline{I}_P} = \frac{\Delta \underline{I}}{\underline{I}_P}, \tag{8.8}$$

where ratio $k_{In} = 1$.

Because in this system the indirect comparing is realized, then equation (8.8) is

$$\delta \underline{I} = \frac{\frac{\Delta \underline{U}_N}{R_{N1}}}{\frac{\underline{U}_P}{R_N}} = \frac{\frac{\Delta \underline{U}_{N1} + \Delta \underline{U}_{N2}}{R_{N1}}}{\frac{\underline{U}_P}{R_N}} = \frac{\Delta \underline{U}_{N1} + \Delta \underline{U}_{N2}}{\underline{U}_P}, \tag{8.9}$$

where $R_{N1} = R_N$.

Resistor R_{N2}, connected to auxiliary CT T_2 secondary circuit has a value $R_{N2}=R_{N1}=R_N$.

Voltage difference, which is characterizing the CT error

$$\Delta \underline{U}_N = \underline{I}_{S1} R_{N1} + \underline{I}_{S2} R_{N2} - \underline{I}_p R_N . \tag{8.10}$$

Errors of a main CT (δI_{X1}) and auxiliary CT (δI_{X2})

$$\begin{aligned} \underline{I}_{S1} &= \frac{\underline{I}_p}{k_N}\left(1 + \delta \underline{I}_{X1}\right), \\ \underline{I}_{S2} &= \frac{\underline{I}_p - \underline{I}_{S1}}{k_N}\left(1 + \delta \underline{I}_{X2}\right), \end{aligned} \tag{8.11}$$

after simple transformation the (8.10) is

$$\Delta \underline{U}_N = \underline{I}_p\left(1 + \delta \underline{I}_{X1}\right) R_{N1} + \underline{I}_p \delta \underline{I}_{X1}\left(1 + \delta \underline{I}_{X2}\right) R_{N2} - \underline{I}_p R_N . \tag{8.12}$$

Because resistors values R_N, R_{N1}, R_{N2} are each equal, then the equation describing a voltage drop characterizing CT error is

$$\Delta \underline{U}_N = -\underline{I}_P R_N \delta \underline{I}_{BH}, \tag{8.13}$$

where $\delta \underline{I}_{BH} = \delta \underline{I}_{X1} \delta \underline{I}_{X2}$.

Replacing the equation (8.13) with (8.10)

$$\delta \underline{I} = -\delta \underline{I}_{BH} . \tag{8.14}$$

This relation shows that the Brooks-Holtz CT error is proportional to main CT error $\delta \underline{I}_{X1}$ and auxiliary CT errors $\delta \underline{I}_{X2}$ product.

Voltage $\Delta \underline{U}_N$ is balanced by the $\Delta \underline{U}_k$ voltage, obtained out of voltage divider, created from r_1, r_2 resistors, conductance G, capacitor C and inductive voltage divider IVD. When the ratio is equal $k_{In} = 1$, then this voltage is described by

$$\Delta \underline{U}_k = \underline{I}_P r_1 \left(\frac{r_2}{\frac{1}{G} + r_2} + \frac{r_2}{\frac{1}{j\omega C} + r_2} \right) \approx\sim \underline{I}_P r_1 r_2 \left(G + j\omega C \right), \tag{8.15}$$

where 1/G » *r*2 i 1/(jωC) » r_2.

From relations (8.9) and (8.15) the expression describing a tested CT error can be calculated from

$$\delta I = \frac{r_1 r_2}{R_N} \left(G + j\omega C \right). \tag{8.16}$$

The tested CT current error

$$\delta I = -\frac{r_1 r_2}{R_N} G \tag{8.17}$$

and angle error

$$\gamma = \omega \frac{r_1 r_2}{R_N} C \,. \tag{8.18}$$

To sum up the properties of a current transformers it can be written that:

- It provides galvanic isolation,
- the magnetic current i_0 causes error reconstruction of every discrete-time current value,
- zero current by zero value delay is present,
- none information is transferred about constant current component,
- limited linear range processing,
- there is a possibility of ambiguous current processing after high pulse current transition,
- CT has to work with closed secondary circuit

The sensor circuits are inductively coupled by a magnetic flux proportional to the current process. The signal induced in the output circuit sensor is exactly proportional to the derivative of current and the coefficient of proportionality is constant for any value of current over a wide frequency band.

Inductive sensors are used to process the current network, but only in the form of a flexible Rogowski coil, which can include cables leading current. Rogowski coil does not provide the exactly even distribution of coils on a closed circuit, which means that in the coil can induce extraneous signals from interfering fields. The sensor with homogeneous magnetic circuit has a higher accuracy of processing, but its installation is necessary to interrupt circuit current processed.

On the ring with a precise and constant cross-section dimensions (Fig. 8.5) wound with possibly even two layers of wire in isolation. The first layer was wound tightly on coiled filled inner circumference of the ring, twice shorter than

the outer perimeter. In this way, the outer perimeter was filled with a layer and at the periphery of the inner-two. The magnetic field generated by current is eddy. The magnetic field intensity is described by basic equation

$$\oint H_l dl = i_1 N_1, \tag{8.19}$$

where: H_l - component of field intensity tangential to the closed path consisting of N_1 turns leading the same current i_1. The magnetic flux field strength derived from the H_l is associated with the sensor windings and the number of turns N_2 is proportional to the current i_1.

$$\psi = M i_1, \tag{8.20}$$

and the proportionality factor is

$$M = \mu_0 \frac{N_1 N_2}{2\pi} \int_{y_1}^{y_2} \ln \frac{r_2(y)}{r_1(y)} dy . \tag{8.21}$$

Occurring in equation (8.21) the functions $r_1(y)$ and $r_2(y)$ describe the cross-boundary sensor. In the particular case, if the cross section is a rectangle with width b, then

$$M = \mu_0 \frac{N_1 N_2}{2\pi} b \ln \frac{r_2}{r_1} . \tag{8.22}$$

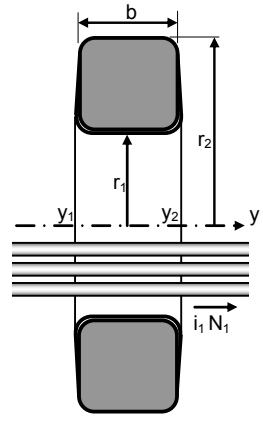


Fig. 8.5. An inductive sensor with a homogeneous magnetic circuit

Processing coefficient depends only on fixed parameters. It does not depend on the configuration circuit or on external magnetizing fields, but only if the coils are accurately N_2 spread evenly on the circumference of the ring and when the accidents are compensated loops that make up the various layers of the sensor windings. Scrolls of the primary current can, in principle, be bent freely. Equitable distribution of the primary coil is preferred. Produced by primary current magnetic

field is then approximately perpendicular to the secondary coils, so the component of the electric field perpendicular to the coils is close to zero, which greatly reduces the impact of capacity between the coil on the accuracy of processing.

To determine the overall dependence of processing on the dimensions of the sensor, it should be fixed and the density distribution of coils on the outer circumference of the ring is

$$\nu = \frac{N_2}{2\pi r_2} = const\ . \tag{8.23}$$

Equation (8.22) is then transformed into

$$M = \mu_0 \nu N_1 r_2 b \ln \frac{r_2}{r_1}\ , \tag{8.24}$$

from which it follows that the processing rate is greater the larger the sensitivity of the sensors.

On the basis of the output signal from the sensor

$$e_2 = -M \frac{di_1}{dt} \tag{8.25}$$

a designation series of instantaneous current i_{1k} by measurement the average value of the pieces cut from the selected signal to the moments t_k moments after half $t_k + T/2$ can be done

$$\overline{E}_k = \frac{1}{T_c} \int_{t_k}^{t_k+T/2} e_2\, dt = \frac{2M}{T_c} i_1\left(t_k\right), \tag{8.26}$$

where $T_c \geq T$ – time averaging (integration). Equation (8.26) is valid under the assumption that the line current i_1 is symmetric, when

$$i_1\left(t_k\right) = -i_1\left(t_k + T/2\right). \tag{8.27}$$

Moreover, if the current i_1 is in galvanic isolated circuit, it is in a similar way to synchronously determined sequence of instantaneous load, by measurement the average half-cut parts of the periodic voltage drop caused by the current i_1 to the resistor R

$$\overline{U}_k = \frac{2R}{T_c} q_1\left(t_k\right). \tag{8.28}$$

Strings averages $\overline{E}_k$ i $\overline{U}_k$ form the coordinates $\overline{E}$, $\overline{U}$ loop (Fig.8.6). The surface of the loop is proportional the square of the RMS current i_1

$$I_1^2 = \frac{T_c^2}{4MRT} A_{\overline{E},\overline{U}}\ . \tag{8.29}$$

$A_{\overline{E},\overline{U}}$ surface can be accurately determined by the estimator

$$A_{\overline{E},\overline{U}} = \sum_{k=1}^{n-1}\left(\overline{U}_{k+1} - \overline{U}_k\right)\frac{\overline{E}_k + \overline{E}_{k+1}}{2} + \left(\overline{U}_1 - \overline{U}_n\right)\frac{\overline{E}_1 + \overline{E}_n}{2}, \qquad (8.30)$$

which does not require that the measurements were carefully spread over the period.

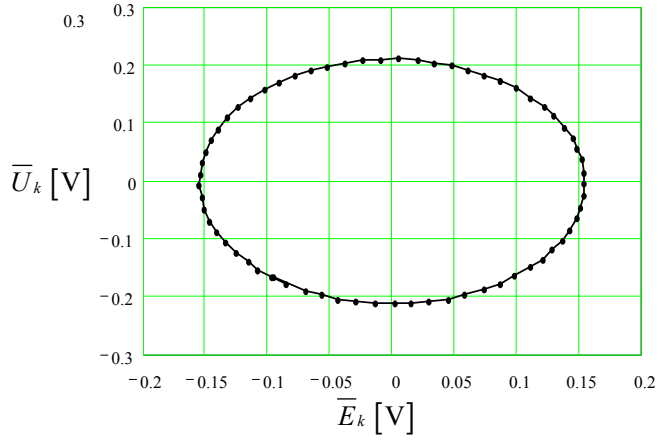


Fig. 8.6. Loop created by the sequence steam value of $\overline{E}_k, \overline{U}_k$

In addition, loop area does not depend on the constants, which may arise as a result of signal processing and the course of the loop can be accurately determined even with small fluctuations in the current network.

Inductive sensor converts the AC voltage signal induced in the circuit galvanic insulated from the circuit. The signal is exactly proportional to the derivative of the current and the proportionality factor is constant for any currents. Differential dependence of the signal from the current causing the current needed to restore operations is the implementation of integration or averaging, taking into account the initial condition. Because this sensors have a voltage output signal, then can be used directly in digital measurement circuits to measure currents, active and reactive power.

Inductive sensor with homogeneous magnetic circuit cannot be installed in the current circuit without interruption.

8.2. SMART SENSORS

Classical integrated sensor is shown in Fig. 8.7a. Build of this sensor presents four main components: sensor (resistor, thermistor, photodiode, capacitor), conditioner, where the sensor output signal is processed (linearization, filtering,

amplifying). If in the system more than one sensor is present, then those signals are multiplexed before A/D conversion process. After digitizing operation the signal is transmitted (by wire or wireless interface) to control system (for example industrial computer unit).

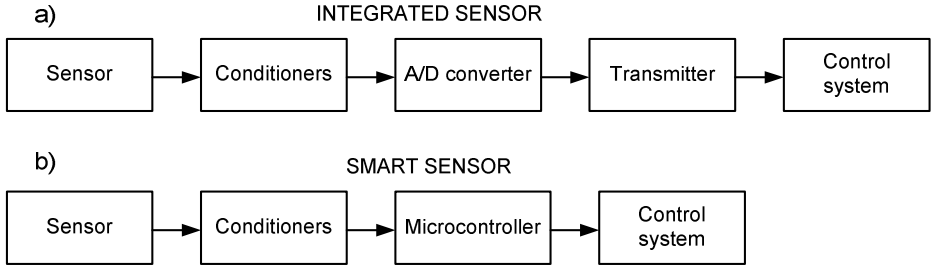


Fig. 8.7. Difference between a) an integral and b) a smart sensor

Other sensor structure, known as smart sensor is presented in Fig. 8.7b. Sensor output signal after being preliminarily processed is fed to the microcontroller. Microcontroller ensures conversion of analog signal into digital one, signal analyzing and standard communication interface to communicate with connected devices. In microcontroller memory the logical functions, which are responsible for sensor intelligence, can be built in. For example there can be such additional functions built in: auto calibration, auto diagnostics. The typical structure of smart sensor is shown in Fig. 8.8. Modern digital measurement systems consist on many sensors. Transducers are known as a smart measurement systems. Single sensors in complex systems could be responsible for measurement of the same or different physical quantities – then they represent a sensors matrix.

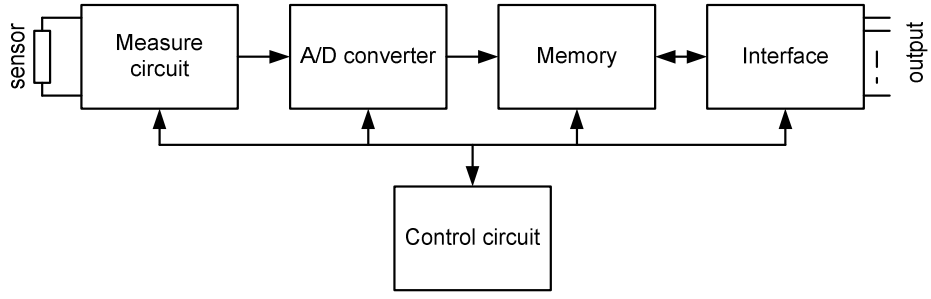


Fig. 8.8. A smart sensor typical internal structure

In the comparison with classic solutions presented in table 8.1, smart sensors can realize such tasks as:

- processing characteristics linearization – using algorithms and data coming from built-in compensatory sensors or from primary (superior) system,

increase measure precision and eliminate influence of such factors as temperature or pressure,
- error detection and diagnostics,
- two-way devices communicating in network,
- autotest and autocalibration - the possibility of sensor remote control,
- acquisition and analysis of the measurement data – using built-in memory, microprocessor and network communication device,
- ability of learning and independent decision making – e.g. choosing of the measurement range.

In industrial measurement solutions there can be found multiple networks and sub-networks. Modern smart sensors are "plug and play" compatible with all different field and device networks. The international standard IEEE 1451.2 says, that sensor interface standard is to make network independent sensors. Fig. 8.9 shows the basic components of an IEEE 1451.2 compatible system [7].

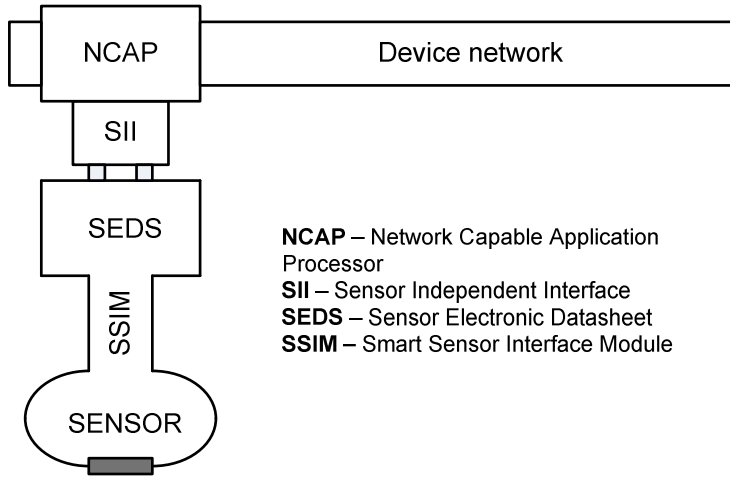


Fig. 8.9. Standardization of smart sensor interfaces

Industrial networks can take many forms. The device network in Fig. 8.10 represents network such as Ethernet. A device network by this definition is not generally intended to interfere directly with a smart sensor. A network connected to branch is intended specifically to interfere with smart sensors. Most networks like CAN-bus and HART also provide power to smart sensors.

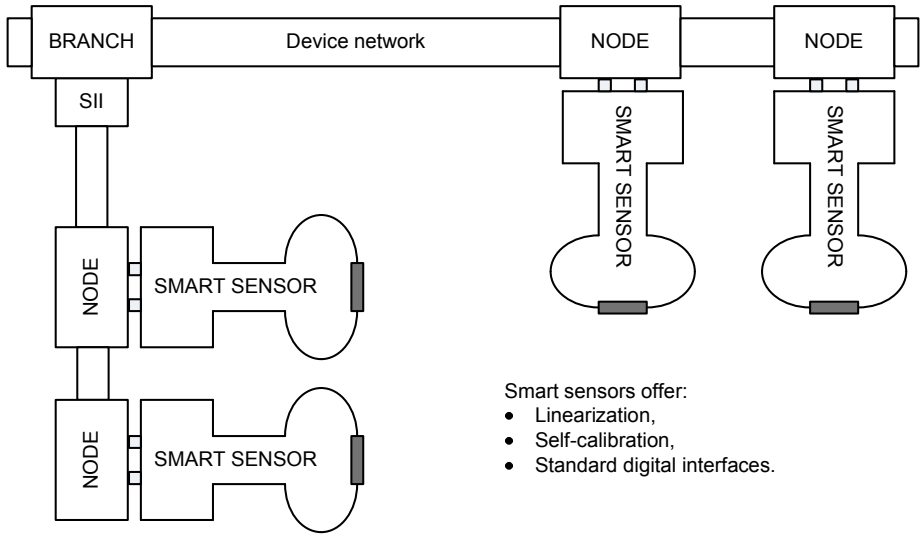


Fig. 8.10. Smart sensors industrial networking

The smart sensor is referred as a *SSIM* (Smart Sensor Interface Module). It contains one or more sensors in addition to any signal conditioning and A/D or D/A conversion required to interface the sensor with a microcontroller. The microcontroller has access to memory that contains a *SEDS* (Sensor Electronic Datasheet) field, which stores sensor specifications. The network capable application processor is basically a node on the network to which a SSIM can be connected. *SII* (Sensor Independent Interface) is responsible for connection between the sensor and the *NCAP* and allows any *SSIM* to be plugged into any NCAP node on any network as it is shown in Fig. 8.11.

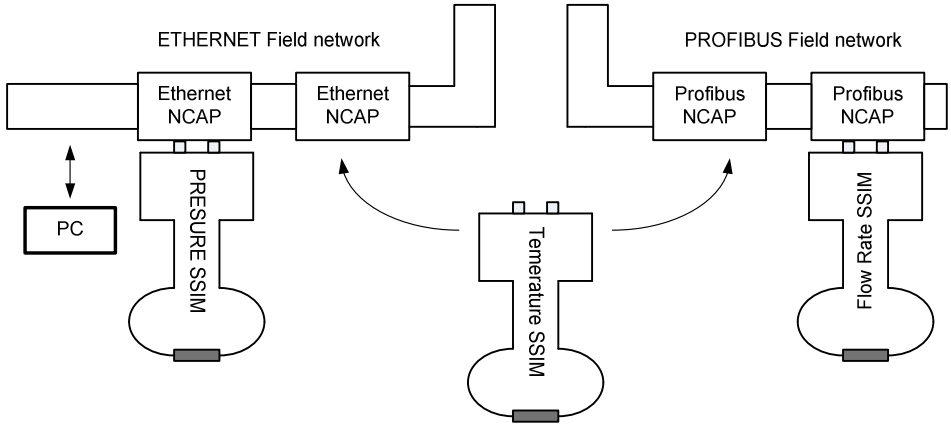


Fig. 8.11. True plug and play network

When the smart sensor is for the first time connected to new network, the digital information from the sensor interface module is available to the network. This information is needed to identify:

- type of sensor which has just been connected,
- available input and output data,
- the units of input and output data,
- the specified accuracy of the sensor,

and various other information about the sensor. That solution gives time savings because the process of added or replaced sensor configuration is done automatically. True plug and play performance with network is possible.

Most smart sensors contain the primary components shown in Fig. 8.12. The MicroConverter (Analog Devices) products are the first to incorporate all of these components on a single chip as it is shown in Fig. 8.13.

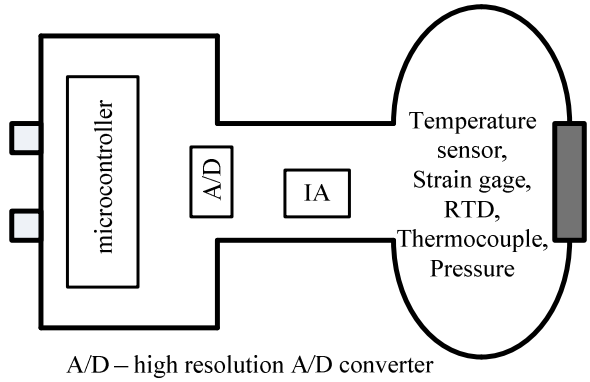


Fig. 8.12. A typical smart sensor

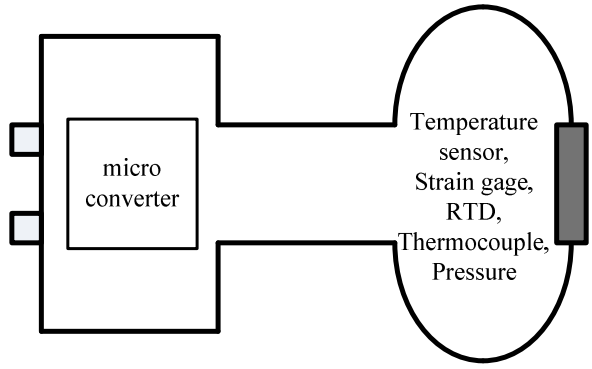


Fig. 8.13. A smart sensor with a MicroConverter

The three main functions of every MicroConverter product are:

- high resolution A/D and D/A conversion,
- flash EEPROM memory for program and data storage,
- microcontroller.

Fig. 8.14 shows a 4-20 mA output of smart sensor which is completely powered by the loop power supply. The used internal 4-20 mA current, as well as the rest of the return current, flows through the R_{SENSE} resistor. The sensing circuit compensates return current and ensures that the actual loop return current corresponds to required by the digital code applied to the D/A converter through the microcontroller. The sensor output can be digitized by sigma-delta A/D converter. The total current value, required by all the circuits under loop power, is less than 4mA maximum value. The D/A converter for circuit shown in Fig. 8.14 must contain a regulator circuit which controls the gate of the external FET transistor.

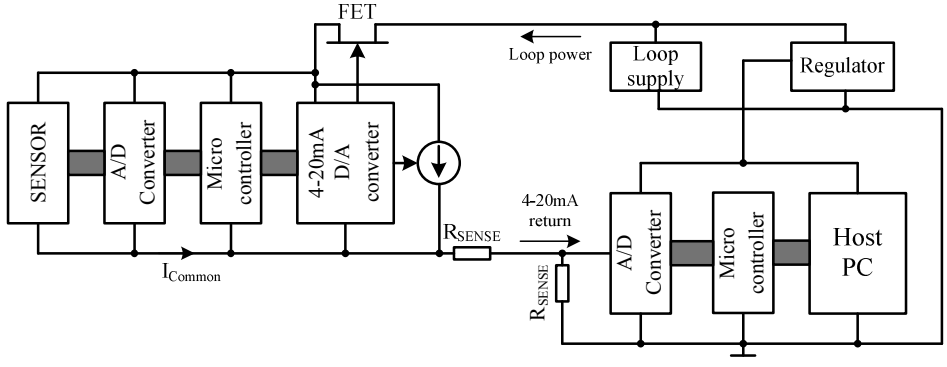


Fig. 8.14. A 4-20mA loop supplied smart sensor

The application of sensors in a typical process control system is shown in Fig. 8.15. Assume the physical property to be controlled is the temperature. The output of the temperature sensor is conditioned and then digitized by an A/D converter. The microcontroller or host computer determines if the temperature has proper value and outputs a digital word to the D/A converter. The D/A converter output is conditioned and drives the actuator (heater).

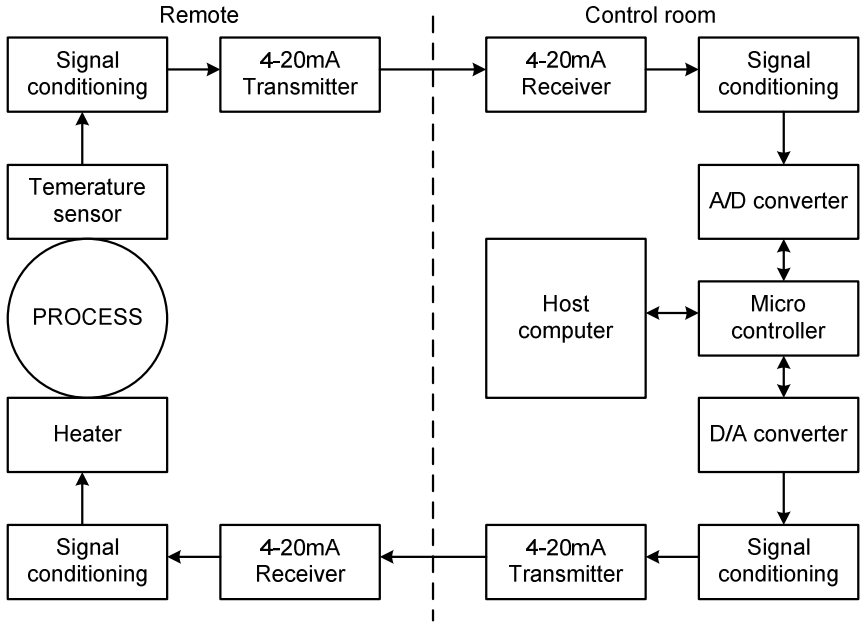


Fig. 8.15. A typical industrial control loop

9. WIRELESS STRAY MEASUREMENT SYSTEMS

In general case the stray measurement systems can be designed as a wire, wireless and very often as a mixed. Stray measurement system division is shown in Fig. 9.1. In this book a chosen stray wireless measurement systems was discussed, more information about wired measurement systems can be found in [24, 31].

Wireless communication offers many benefits for measurement applications used in renewable energy systems. The general benefit of stray wireless measurement systems is minimization of wires and cables usage. Because renewable energy sources very often are strayed on a huge space, so physical wiring can be expensive (depends on used wires interface standard) and sometimes even impossible. Wireless measurement systems extends the distance, or range, of data transmission to specialized measure-control systems. Large scale systems, such as stray wind power plant, widely use wireless technologies. The benefit is that it has low installation operating costs, but the disadvantage is a higher purchase cost. Stray measurement systems are designed for a long working time, so the total cost of using wireless measurement system is almost always lower.

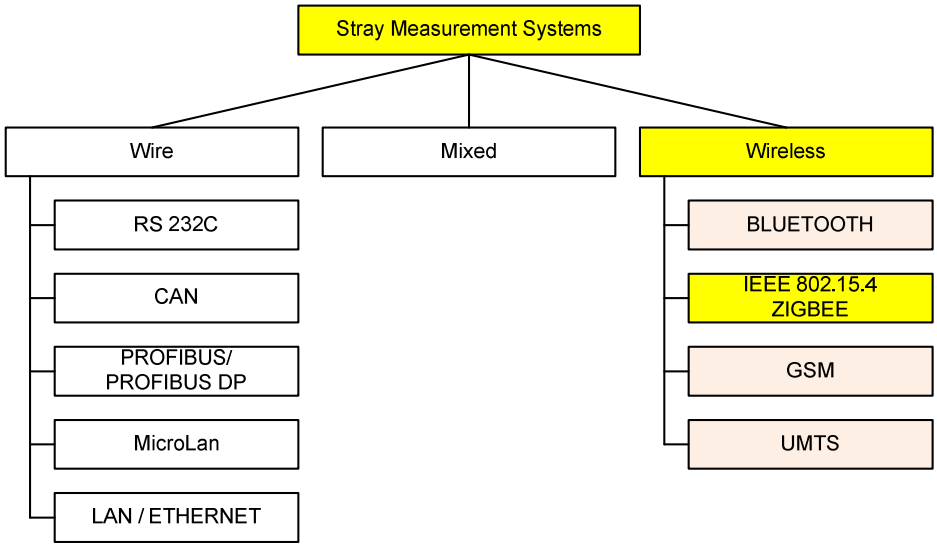


Fig. 9.1. A division of the stray measurement systems

To correct design a stray wireless system the designer should have knowledge about the parameters of the measured signal sources. In this case that will be the renewable energy sources. To the parameters it can be listed: the distance, data rate (data transmission speed), number of receivers and transmitters and the wireless interface compatibility. The important problem is a wireless network security. To secure important measurements and control information a few methods are used

today. To the most popular can be listed a security protocols used in IEEE 802.11 standard, or security protocols used in other standards like Bluetooth, IEEE 802.15.4. Another security measure is to minimize the propagation of radio waves outside the physically controlled area of a facility. This causes the wireless network to be more secure.

Very popular method today is a sending measure data by GSM protocols. The Table 9.1 presents the different transmission modes used in telecommunication networks. It is a very big advantage, that the measurement information can be sent on unlimited distances. The disadvantage is, that user or operator must pay for the data transmission.

Table 9.1. The GSM transmission modes

Transmission mode	Description	Maximum data transmission speed	Telecommunication network
CSD	Standard digital data transmission	9.6 kb/s	GSM
CSD	Digital data transmission with data compression	14.4 kb/s	GSM
HSCSD	Fast digital data transmission	57.6 kb/s	GSM + small modifications
GPRS	Package data transmission	115 kb/s	GSM + GPRS framework
EDGE	Better data transmission in modified GSM network	384 kb/s	GSM + large modifications
UMTS	UMTS transmission data	1960 kb/s	Global UMTS network

How to design a wireless measurement system is presented in Fig. 9.2.

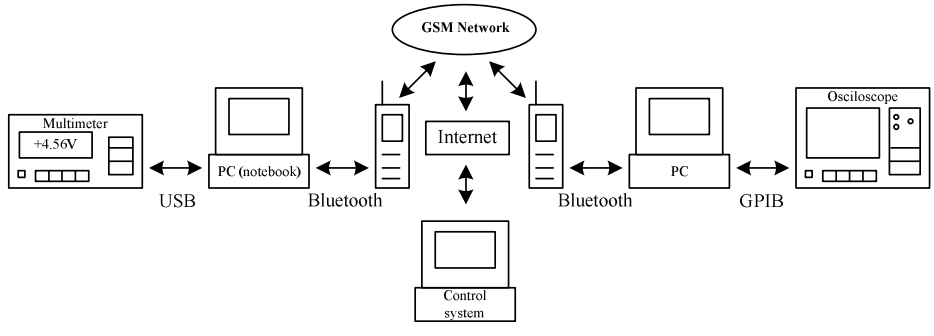


Fig. 9.2. A block diagram of the stray GSM measurement system

The real instruments as the multimeters, oscilloscopes, analyzers can be replaced by virtual instruments built on the base of data acquisition cards. The measurement results, or measurement results and analysis results in case of virtual instruments, can be transmitted through the device with GSM module by the GSM network directly to the control system. The transmission can be bidirectional, that is a control and measurement system, or only one way transmission, then it is a measurement system. The GSM measurement system algorithms usually are not very complicated. First of all, the system must know what to do, so the control station usually has two work modes: transmission and monitoring, the instrument has two modes too: can work as a remote device or local device. The full algorithm of GSM basic transmission is presented in Fig. 9.3.

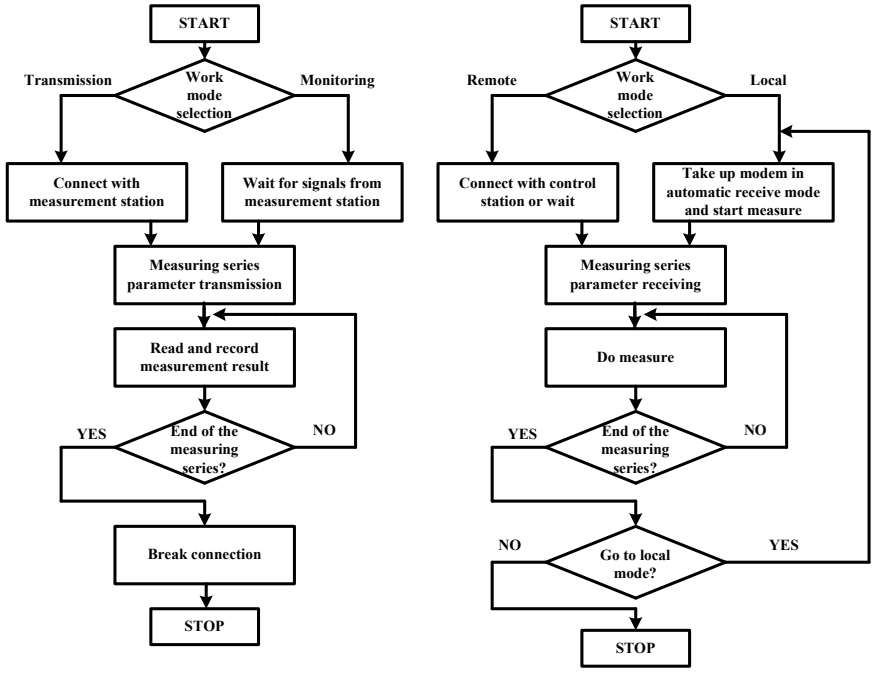


Fig. 9.3. A transmission algorithm of a GSM measurement system

However, sending of the information by the GSM modules is very easy, sometimes it is better, especially for shorter distances, to use other wireless interfaces. Bluetooth interface is very often used in GSM measurement systems to connect the computer (notebook with installed Bluetooth module) and a mobile phone as it is shown in Fig. 9.2. But sometimes it is needed to build a uncomplicated measurement system, i.e. with multimeter and a work station to do some analysis. Moreover the results of measurement and analysis has to be sent to the control station and printed in order to archive. Then the ideal solution is presented in Fig. 9.4, usage of the Bluetooth wireless interface.

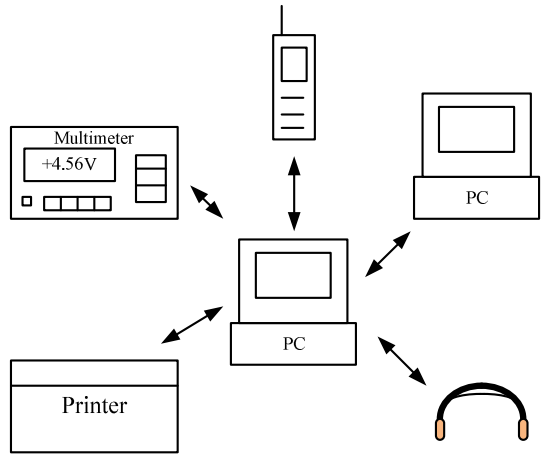


Fig. 9.4. A bluetooth measurement system

It could be a problem when more than seven devices must be connected to Bluetooth module which is working as a master device, because the maximum number of devices cannot be higher than 2^3, that is 8 with a master device. At that application one more master device must be added. The first master device will be working as a slave device to the second master Bluetooth device as it is shown in Fig. 9.5.

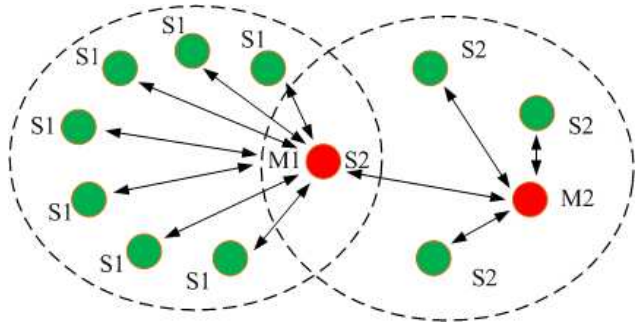


Fig. 9.5. An extended Bluetooth measurement network

Measurement information from the S1 devices are transmitted through their master device M1 to se second master device M2. The main master device is now the M2 device. Because the data rate is limited, the information density from S1 devices could not be too high. To name a disadvantage, the high power consumption can be listed. Bluetooth device should be powered all the working time, because the launching time is long and equal 3 seconds. The application of using Bluetooth device is shown in Fig. 9.6 and 9.7. Fig. 9.6 presents the basic acquisition system consisting of a multimeter to acquisition data and a computer to analyze data. The transmitter and receiver can communicate on a maximum

distance up to 100m. Some older Bluetooth devices can communicate only in distance up to 10m (important for older notebooks).

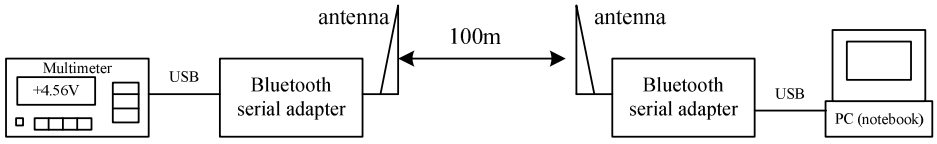


Fig. 9.6. Basic Bluetooth measurement system

Fig. 9.7. shows the data acquisition card with Bluetooth interface and two sensors. This solution is nowadays more often used, because it can use smart sensors directly.

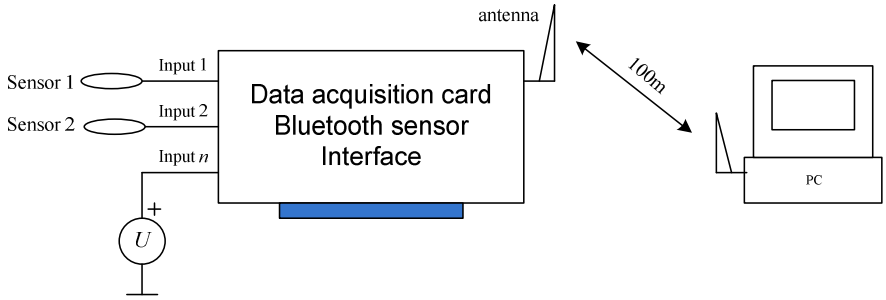


Fig.9.7. DAQ card measurement system

For the measurement-based applications there is also IEEE 802.15.4, known as ZigBee standard. Works on this standard have been done since 2000. ZigBee has lower bandwidth than Wi-Fi but has longer range, requires lower power and network can be configured as the mesh networking topology. This solution is used for long-term measurement applications, like monitoring batteries voltage [37].

Features of IEEE802.15.4 standard

- low power consumption – ZigBee standard is designed to work with battery supply,
- ZigBee has two basic modes: active (transmit/receive) or sleep,
- even mains powered equipment needs to be conscious of energy. Consider a future home with 100 wireless control/sensor devices:

1. 802.11 Rx power is 667 mW (always on)@ 100 devices/home & 50,000 homes/city = 3.33 megawatts.
2. 802.15.4 Rx power is 30 mW (always on)@ 100 devices/home & 50,000 homes/city = 150 kilowatts.
3. 802.15.4 power cycled at .1% (typical duty cycle) = 150 watts.

ZigBee devices will be more ecological than its predecessors, saving megawatts at it full deployment.

- low cost (device, installation, maintenance),

- high density of nodes per network,
- simple protocol, global implementation.

General characteristics of IEEE 802.15.4:

- dual physical layer (2.4GHz and 868/915 MHz),
- data rates of 250 kbps (@2.4 GHz), 40 kbps (@ 915 MHz), and 20 kbps (@868 MHz),
- optimized for low duty-cycle applications (<0.1%),
- yields high throughput and low latency for low duty cycle devices like sensors and controls,
- multiple topologies: star, peer-to-peer, mesh,
- addressing space of up to: $18.45 \cdot 10^{+18}$ devices (64 bit IEEE address), 65535 networks,
- fully hand-shaked protocol for transfer reliability,
- range: 50m typical (5-500m based on environment).

Fig. 9.8 shows ZigBee network model.

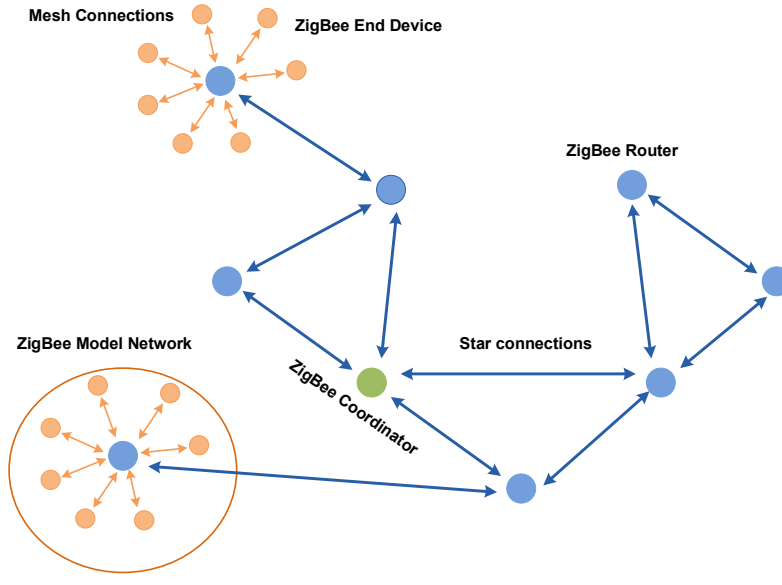


Fig. 9.8. ZigBee network model

The ZigBee coordinator has to set up a network, transmit network beacons, store node information and route signals between paired nodes. Network Coordinator usually operates in the receiver mode. Because ZigBee standard is similar to the Bluetooth standard, then the usage comparison between those two standards can be done.

Bluetooth standard can be used in following applications:

- synchronization of cell phone to PDA,
- hands-free audio,
- basic measurement systems.

ZigBee is better suited for:

- **controls,**
- **sensors,**
- lots of devices,
- low duty cycle,
- small data packets.

It is very interesting how the data size influences the effective network communication transfer function. It was tested in the system shown in Fig. 9.9.

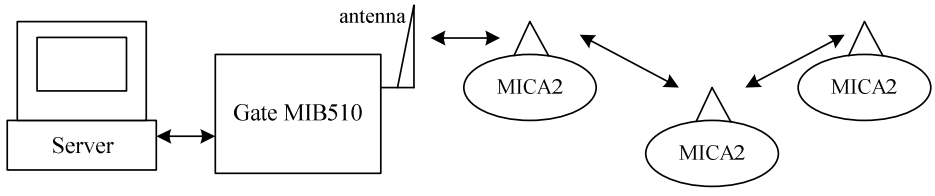


Fig. 9.9. ZigBee test measurement system

In this measurement system the measurement server connected with MIB510 gate (interface RS232), the place where ZigBee coordinator and three Mica 2 modules are mounted, which are working as a router is present. System working frequency is 915MHz, but maximum data rate for this module is only 19.6 kb/s. Results presented in Fig. 9.10 are mean values from 1000 tested elements. The research was done for transmission protocol without data verifying.

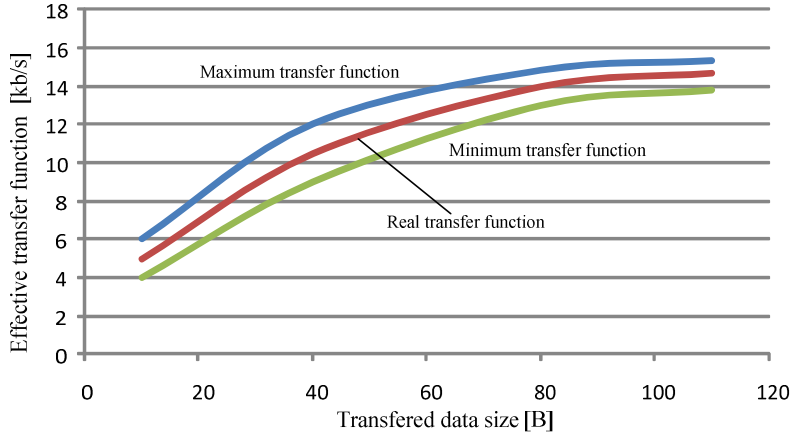


Fig. 9.10. Effective network communication transfer function

The second part of the test was a obstacle impact on effective network communication transfer function. The results are presented in Fig. 9.11.

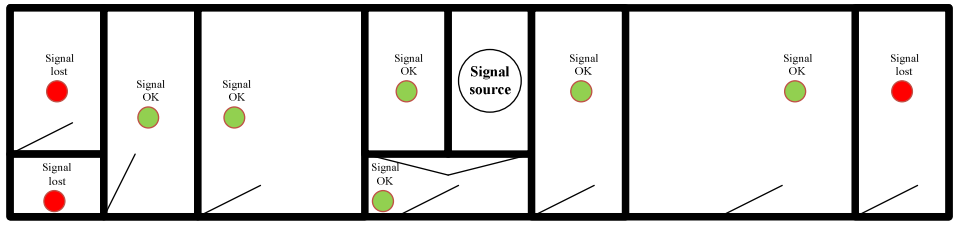


Fig. 9.11. Obstacles impact on data rate

The results are very interesting, because when the ZigBee device can make stable connection to the other ZigBee devices, the signal was transferred with full data rate. When the connection was lost, all the data and signal was lost.

To sum up this chapter the table 9.2 presents a comparison of short range radio transmission systems.

Table. 9.2. Comparison of short range radio transmission systems

Interface	Bandpass	Transmission speed	Linear range	Max network nodes	Time to get number of new device	Device activation time
Bluetooth	2.45GHz	1Mb/s	10m (100m)	8	3s	3s
ZigBee	868MHz 915MHz 2.45MHz	20kb/s 40kb/s 250kb/s	100m 100m 50m	65536	30ms	15ms
Home RF 1.0 Home RF 2.0	2.45MHz 2.45MHz	2Mb/s 10Mb/s	50m 50m	128	No data	134us
Area Infra Red		4Mb/s	8m	10	No data	No data
Hiperlan 2	5.2GHz	54Mb/s	150m	10	No data	No data

10. VIRTUAL INSTRUMENTS

Virtual instruments are presenting, after analog and digital instruments, new class of measurement instruments. Digital instruments, sometimes named by system instruments, have digital interface to communicate with computer measurement system. Reading errors in that systems are eliminated and the measurement process is automated. The newest class of measurement instruments presents virtual instruments. In the Virtual Instruments (VI) hardware functions execution is done by the software implemented in personal computer. The main function is control instruments and signal processing algorithm execution, which can be changed by easy way. Virtual Instruments could represent most real instruments from most popular like voltmeters, ohmmeters, oscilloscopes, to more complicated instruments like signal analyzer, signal register, power analyzer or other measurement systems like digital system to tests instrument transformers. The definition of Virtual Instruments might be written as:
Virtual Instrument (VI) it is a kind of intelligent measurement device, which is constructed with combination of new generation hardware, personal computer and friendly for users software. This software must be written so that the functions of real, traditional measurement device were kept [29].

Virtual instruments can be divided into 3 groups:

- type A – graphical panel displayed on monitor imitating and control autonomic real device connected with PC by standard interface – RS232, RS485, IEC-625 or IEEE-488 (GPIB), USB, LAN.
- type B - graphical panel displayed on monitor built with using of data acquisition card.
- Type C - graphical panel displayed on monitor, input data are taken from files or are numerical generated

The example of measurement system consist on real instruments with the GPIB interface is shown in Fig. 10.1.

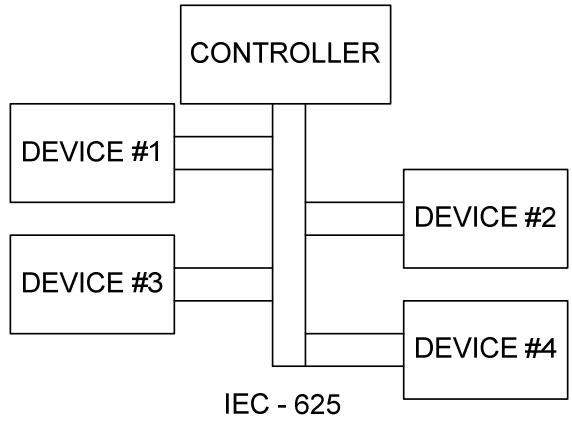


Fig. 10.1. A measurement system with the GPIB interface instruments

The GPIB (General Purpose Interface Bus) interface is a parallel interface which allow to connect instruments, but only in limited distance (short length cables). Usually personal computer fulfill of controller function. Advantage of that solution is an easy possibility of spread out instrument functions.

Fig. 10.2 presents other virtual instrument system - type B.

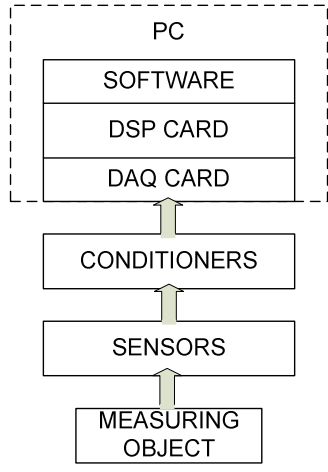


Fig. 10.2. A measurement system with a DAQ card

The first part of this system is analog to DAQ input if in the system the standard analog sensors are used. If in a measurement system the smart sensor with digital data output is used, then the analog line is unnecessary. After conversion the analog signal into digital data in A/D converter (located at DAQ board) the signal can be analyzed and processed. As an effect on the monitor the final measure results are presented.

The generalized measurement virtual instrument system is shown in Fig. 10.3. To VI measurement system can be connected all types of instruments, like autonomous instruments (multimeters, analyzers) connected to directly to measurement object or indirectly by the sensors. Moreover to autonomous measurement devices are numbered among signal generators, power supplies and other specific devices. Specialized industrial measurement systems are built as integrated module instruments with industrial interfaces like VXI (VMEbus eXtensions for Instrumentation) or PXI (PCI eXtensions for Instrumentation [36]). VXI is used in many different applications ranging from test and measurement to data acquisition and analysis in research and industrial solutions. PXI offers a high-performance designing solution for measurement and automation systems. PXI adds mechanical, electrical, and software features that define complete systems for test and measurement, data acquisition, and manufacturing applications [28].

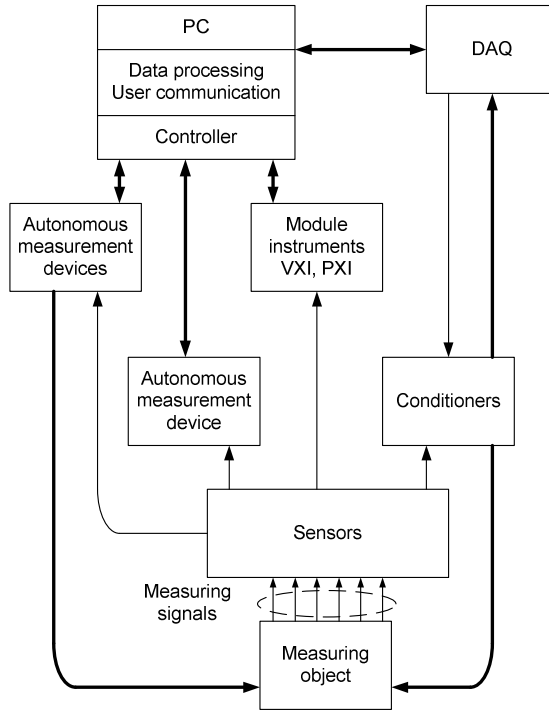


Fig. 10.3. Generalized VI measurement system structure

To calculate VI uncertainties the knowledge about error components is needed. Uncertainty in VIs depends on three components of error:

- error of A/A conversion,
- error of A/D conversion,
- error of D/D conversion.

Parameters characterizes the A/A and A/D conversion error:

- processing resolution,
- zero error of A/D conversion,
- offset,
- gain error ,
- differential and integral nonlinearity,
- reference signal temperature drift,
- noices,
- jitter.

Error of D/D conversion depends on:

- Uncertainty send data processing algorithms,
- Software implementation method (precision of digital processor),
- Uncertainties of measurement data.

Today are two main methods to calculate VI uncertainties:

- Statistical simulation method (Monte Carlo) to calculate the Statistica packet using ability is needed. It often used to complicated measurement system uncertainty analysis.
- Analytical method (ISO recommendation) – used to calculate uncertainty of basic systems consist on a few instruments.

The LabVIEW environment [36]

LabVIEW is a short of Laboratory Virtual Engineering Workbench. It is one of the easiest way to design measurement systems from basic consist on a few measurement devices (meters, DAQ cards) and sensors to large stray measurement systems to measure parameters of solar plant, wind plant and other stray renewable energy sources. LabVIEW is a graphical programming language that uses icons instead of lines of text to create applications. LabVIEW uses dataflow programming, where the flow of data determines execution. The user interface is known as the front panel. Using graphical representations of functions to control the front panel objects you add the code. The block diagram resembles a flowchart. LabVIEW programs are called virtual instruments, or VIs, because their appearance and operation imitate physical instruments, such as oscilloscopes and multimeters. Every VI uses functions that manipulate input from the user interface or other sources and display that information or move it to other files or other computers.

Fig. 10.4 presents the three steps which are needed to correctly design basic measurement system with using of DAQ card [36].

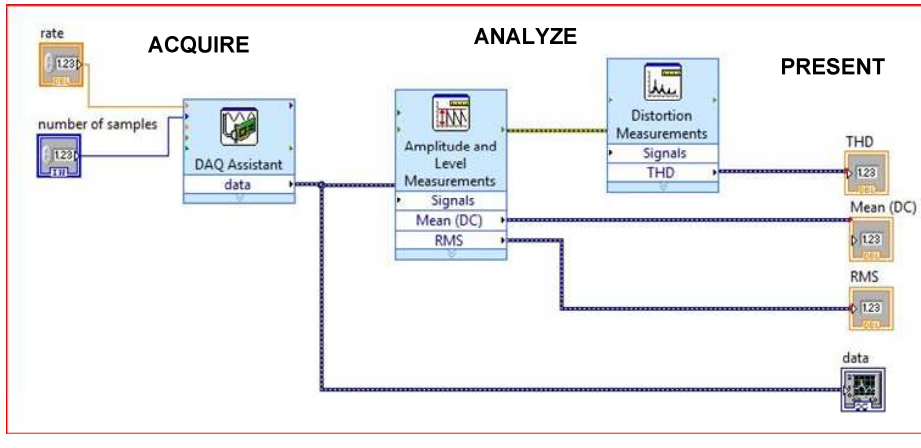


Fig. 10.4. Steps of VI designing

First step is an acquire data from the object. The signal in analog form directly from measurement object or indirectly from the sensor must be adjusted to DAQ card analog input in conditioner circuit. After this operation the signal is converted

to digital data in the A/D converter located on DAQ board. Next the signal can be analyzed. In the example presented in Fig. 10.4 the mean value, RMS value and THD value of acquired input signal is analyzed and calculated. The last step of basic measurement system is a data presentation. In LabVIEW measure data can be presented in a few ways as a numerical (THD, Mean, RMS) or graphical (data) results.

The front panel shown in Fig. 10.5 is built with controls and indicators, which are the interactive input and output terminals. Controls are knobs, dials, push buttons, and other devices. Indicators are graphs, LEDs, and other displays. Controls simulate real instrument input devices and supply data to the block diagram of the VI. Indicators simulate instrument output devices and display data the block diagram acquires or generates.

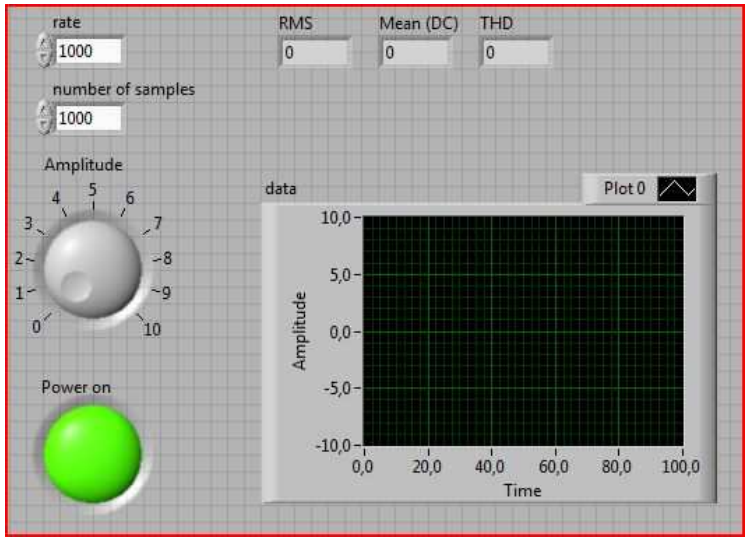


Fig. 10.5. A front panel

The block diagram shown in Fig. 10.6 contains graphical representations of functions source code from the front panel objects. Additionally, the block diagram contains functions and structures from built-in VI libraries. Wires connect each of the nodes on the block diagram, including control and indicator terminals, functions, and structures.

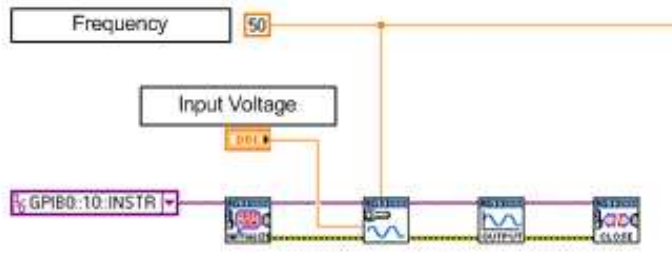


Fig. 10.6. A block diagram

In every programming languages very important thing is a programming structures. Built in LabVIEW programming structures are similar to structures occurring in C++ programming language. Loops are located on the first Functions and next Structures palette located on the block diagram.

The For Loop - executes a subdiagram a set number of times. The sample of this structures is shown in Fig. 10.7.

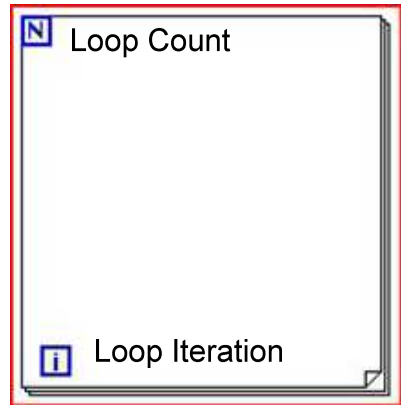


Fig. 10.7. The "For Loop" programming structure

The value in the input terminal indicates how many times to repeat the subdiagram. An output terminal contains the number of completed iterations. The iteration count always starts at zero. During the first iteration, the iteration terminal returns 0.

The While Loop - executes a subdiagram until a condition is met. The example of this structure is presented in Fig. 10.8.

This structure is similar to a *Repeat-Until* loop in text-based programming languages. The *While Loop* executes the subdiagram until the input terminal receives a specific boolean value. The default behavior and appearance of the conditional terminal is *Continue If True*. When a conditional terminal is *Continue*

If True, the *While Loop* executes its subdiagram until the conditional terminal receives a *FALSE* value.

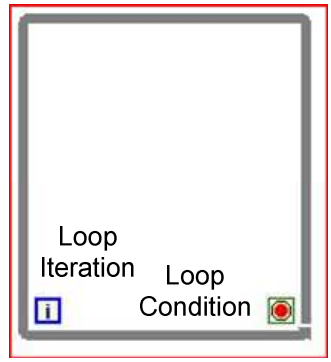


Fig.10.8. The "While Loop" programming structure

The shift registers are using with *For Loops* and *While Loops* (Fig. 10.9) to transfer values from one loop iteration to the next. Shift registers are similar to static variables in text-based programming languages.

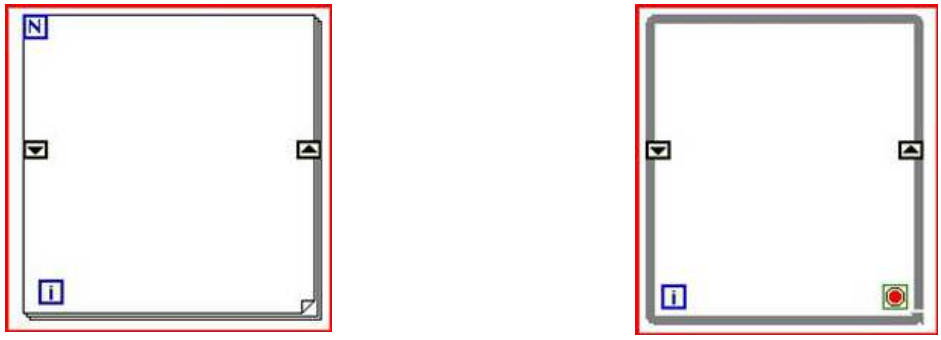


Fig. 10.9. Use of the shift registers with the "For Loop" and the "While Loop" structures

The case structure - contains multiple subdiagrams, only one of which executes depending on the input value passed to the structure. Example of this structure is shown in Fig. 10.10.

The case structure is similar to case statements or if...then...else statements in text-based programming languages.

The case structure has two or more subdiagrams. Only one case is executed at a time. An input value determines which subdiagram executes.

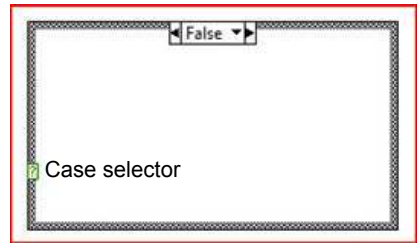


Fig. 10.10. The “Case” programming structure

In this structure only one internal program executes at a time. The value wired to the selector terminal determines which case to execute and can be boolean, string, integer, or enumerated type. This structure gives possibility to make decision in LabVIEW.

Fig. 10.11 presents simple *If Then* case with uses of boolean input: if the boolean input is *TRUE*, the true case will execute; otherwise the *FALSE* case will execute.

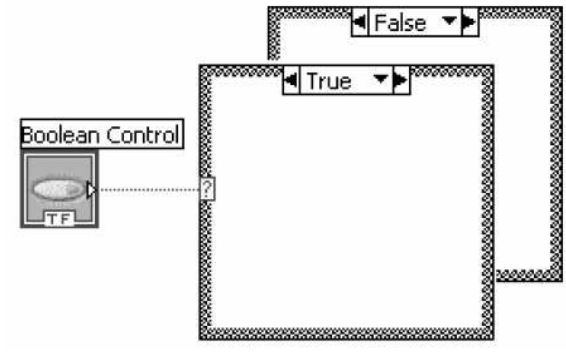


Fig. 10.11. Making decision with use of a boolean input

Fig 10.12 shows the same situation, but with uses a numeric input. The input value determines which box to execute. If out of range of the cases, LabVIEW will choose the default case.

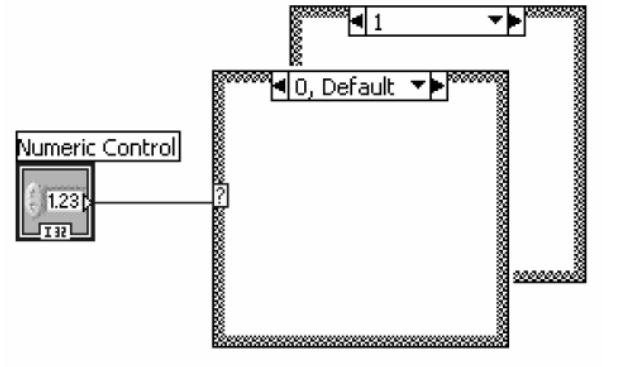


Fig. 10.12. Making decision with use of a numeric input

Fig. 10.13 shows when the boolean passes a *TRUE* value to the select VI, the amplitude value is passed to the indicator. When the boolean passes a *FALSE* value to the select VI, zero is passed to the indicator.

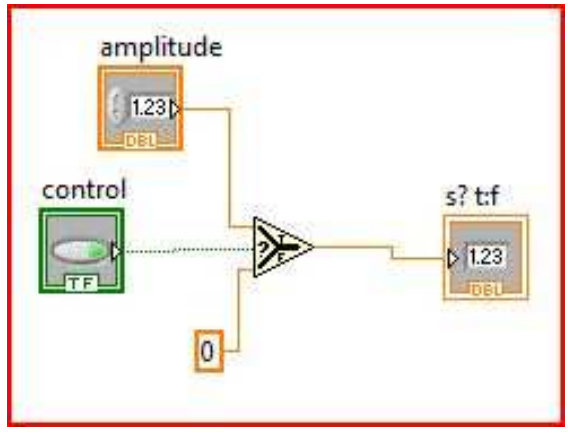


Fig. 10.13. Making decision with use of a select function

The sequence structure - contains one or more subdiagrams, which execute in sequential order (Fig. 10.14).

The sequence structure contains one or more subdiagrams, or frames, which execute in sequential order. The sequence structure executes frame 0, then frame 1, then frame 2, until the last frame executes so it is similar to slide presentation from photo film. The sequence structure does not complete execution or return any data until the last frame finishes.

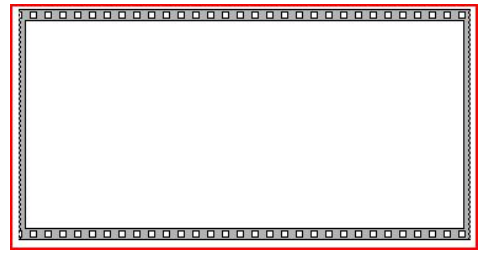


Fig. 10.14. The sequence programming structure

A formula node - performs mathematical operations based on numeric input. The sample of this type of programming structure is presented in Fig. 10.15.

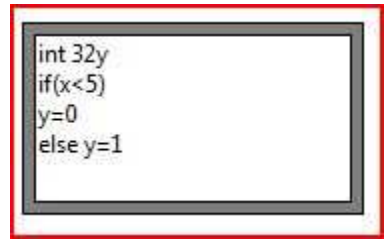


Fig. 10.15. The formula node structure

A formula node is a convenient text-based node you can use to perform mathematical operations on the block diagram. Formula nodes are useful for equations that have many variables or are otherwise complicated and for using existing text-based code.

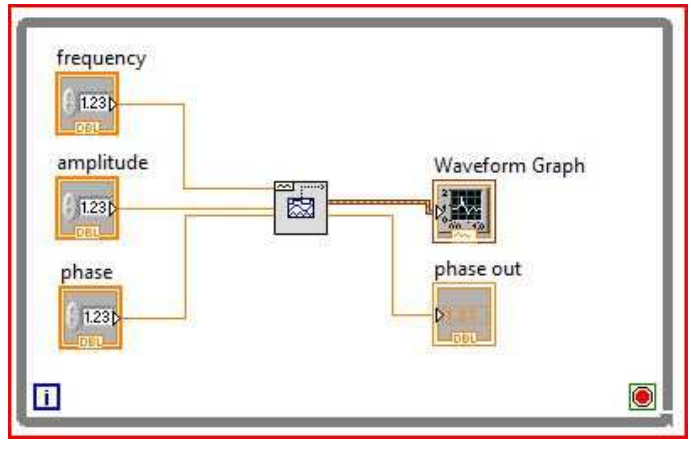


Fig. 10.16. A block diagram of basic VI

Creating new VI in LabVIEW is not very difficult. When an object is creating on the *Front Panel*, then a terminal will be created on the *Block Diagram*. These terminals give access to the *Front Panel* objects from the *Block Diagram* code. Color on the *Block Diagram* provide information about the data type.
The example of basic Vi is presented in Fig. 10.16 – *Block Diagram* and Fig. 10.17 – *Front Panel*.

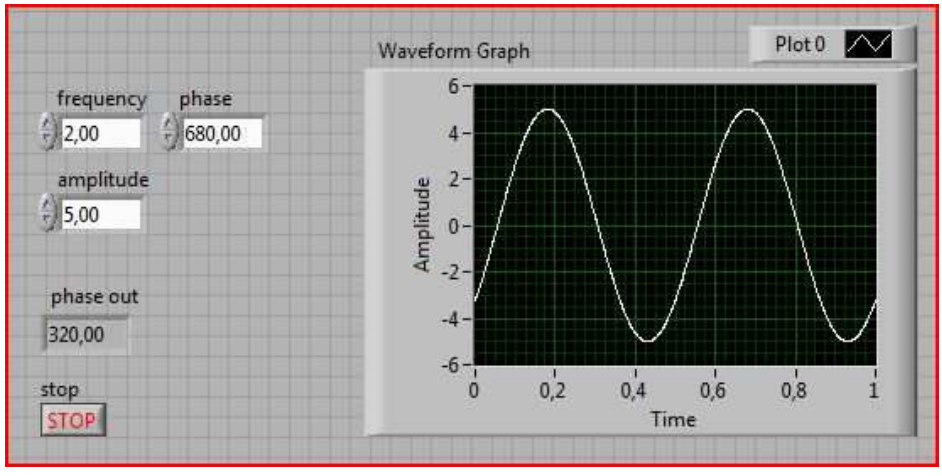


Fig. 10.17. Front panel of basic VI

Sometimes some part of designed VI can be used more than one time. The LabVIEW makes possible to do subVI, as it is shown in Fig. 10.18. In this case program calculate standard and extended uncertainty from *n* samples. Any portion of LabVIEW code can be turned into a subVI. The subVI icons can be modified to more accurately represent the function of the subVI.

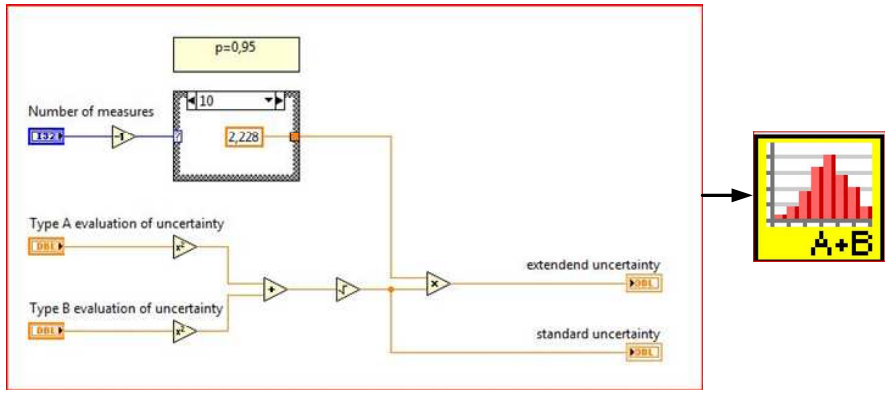


Fig. 10.18. Creating subVI

Instrument control in LabView

All types of instrument can be controlled in LabView with interfaces: serial, parallel port, GPIB, modular instruments (PXI), image acquisition, motion control, USB, ethernet, CAN.

Interface GPIB (General Purpose Interface Bus) is usually used in standalone bench top instruments to control measurements and communicate data. Standards for this interface is defined by IEEE 488.1(2).

Plug and Play drivers are a set of VIs that control a programmable instrument. VIs correspond to instrument operation: configuring, triggering, and reading measurements. Fig. 10.19 presents typical program to read measurement from instrument, in this case multimeter. The blocks on this diagram are drivers for used multimeter downloaded from [36]. If user need some specific instructions then it is possibility to write new driver or change existing. The programming instrument to control needs the same steps as the other programming languages i.e. Agilent VEE. The process first must be initialized then the measurement should be configured (set of resolution, function, range), then the measurement can be read and the result of measurement is presented in *Front Panel.* The last step is close of instrument. Measurement system designer can set more functions and do analysis of measurement results.

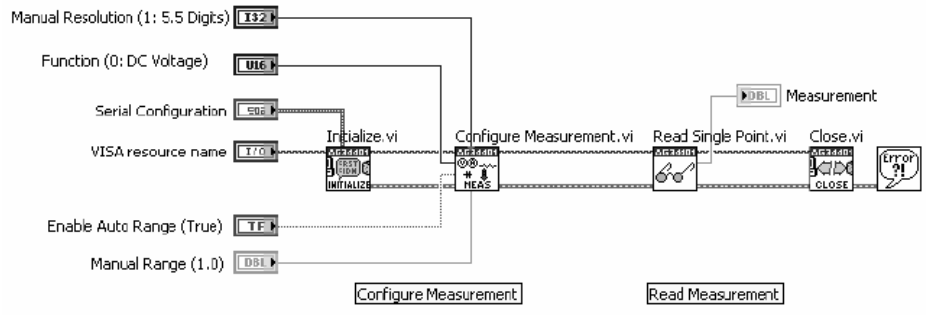


Fig. 10.19. Multimeter measurement process

Methodology of Virtual Instruments designing:

- measure object identification as well as its important parameters,
- selection of proper measurement methods,
- designing and realization of the measurement circuit,
- the study of software and interface to system communication with user,
- instrument calibration,
- preparing documentation.

11. CHOSEN MEASUREMENT SYSTEMS

In case of designing and realization of analog measurement systems, on At the current circuitry technique and technology elements carry out progress stage, two solutions are suggested.

1. In case of measurement line designing it is necessary to use of advanced integrated circuits, like XTR101, XTR102, XTR103, XTR104, XTR100, XTR501 manufactured by Burr-Brown, including transducers cooperating with sensors, normalizing and linearization of the transducers.
2. In case of transducer designing, which is indirect linked between sensor and measurement system, it is necessary to use of instrumentation amplifiers.

Example 1.

Design of measurement line part, from sensor to transducer, doing measure of medium temperature from 0 °C to 400 °C. Output current is changing from 4 mA to 20 mA and it should linear depends from temperature. Measurement line processing error, at line resistance changes (100±10) Ω, should be lower than 0.2 %.

As the temperature sensors can be used thermocouples, thermo resistors (platinum, nickel, copper, thermocouple) and semiconductor junctions. The Pt100 platinum thermo resistor was chosen and XTR103 integrated circuit to this sensor dedicated.

(Comment: If the temperature changes from -100 °C to +200 °C then the best sensor will be the copper thermo resistor – characterizing by linear characteristic in this temperature range).

Platinum sensor can be use in temperature range from -200 °C to +1000 °C. Pt100 resistor has clear-cut described characteristic with relation

$$R_{TD} = R_o\left(1 + At + Bt^2\right), \tag{11.1}$$

where $R_o = 100\,\Omega$,

$A = 3.908 \cdot 10^{-3}\ 1/°\mathrm{C}$,

$B = -0.5802 \cdot 10^{-6}\ 1/°\mathrm{C}$.

Chosen XTR103 transducer include:

- current sources supplying half-bridge consist of R_{TD} resistor and reference resistor R_z,
- instrumentation amplifier,
- linearizator,
- transmitter.

Moreover transducer good feature is, that supplying energy and current signal are transmitted by two-wire line.

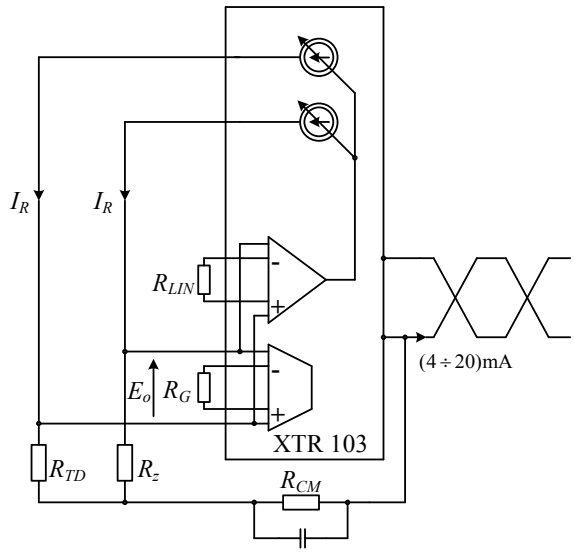


Fig. 11.1. A Pt100 sensor and an XTR103 transducer measurement circuit

Circuit designing is amount to resistances determine: R_G – instrumentation amplifier, R_L – linearizator circuit and supplying voltage U_Z from which depends a measurement line insensitivity on transmission line resistance changing.

Amplifier input voltage described by the relation

$$E_{IN} = E_{IN}^{+} - E_{IN}^{-} = I_R \left(R_{TD} - R_Z \right), \tag{11.2}$$

where: E_{IN}^{+}, E_{IN}^{-} - inverting and non-inverting input voltages,

I_R - current from linearizator controlled source,

R_Z - half-bridge resistance described for initial value of temperature measurement area.

Transducer output current holds

$$I_o = E_{IN} \left(0.016 - \frac{40}{R_G} \right) + 4, \tag{11.3}$$

I_o current is expressed in mA, and resistance of R_G resistor in Ω.

Flowing from linearizator sources currents I_R are described by the relation

$$I_R = I_{R1} = I_{R2} = 0.8 + \frac{E_{IN}}{2R_{LIN}}, \tag{11.4}$$

I_R currents are expressed in mA, E_{IN} voltage in milivolts and resistance of R_{LIN} resistor in Ω.

After insert relation (11.4) into expression (11.2) we got

$$E_{IN} = \frac{0.8\left(R_{TD} - R_Z\right)}{1 - \dfrac{R_{TD} - R_Z}{2R_{LIN}}}. \tag{11.5}$$

After that from relations (11.5) and (11.3) transducer output current was obtained

$$I_D = 0.8\frac{R_{TD} - R_Z}{1 - \dfrac{R_{TD} - R_Z}{2R_{LIN}}}\left(0.016 - \frac{40}{R_G}\right) + 4. \tag{11.6}$$

Current changes will be linear depends on R_{TD} resistance changing where

$$\Delta R_{TD} = R_o\left(1 + At\right) - R_Z = \frac{R_{TD} - R_Z}{1 - \dfrac{R_{TD} - R_Z}{2R_{LIN}}}. \tag{11.7}$$

The derived relations are general relations. If we take data into consideration in this example, then $R_Z = R_o$, temperature $t = t_g$ - upper measure area, and the above equation gets

$$\Delta R_{TD} = R_o A t_g \equiv \frac{R_o\left(At_g + Bt_g^2\right)}{1 - \dfrac{R_o\left(At_g + Bt_g^2\right)}{2R_{LIN}}}, \tag{11.8}$$

and after transformation

$$R_{LIN} = -\frac{1}{2}R_o\frac{A}{B}\left(A + Bt_g\right). \tag{11.9}$$

From equation (11.6) will be determined resistor R_{LIN} resistance of linearizator and according to this task is equal

$$I_{o,\max} = 0.8\frac{R_o\left(At_g + Bt_g^2\right)}{1 - \dfrac{R_o\left(At_g + Bt_g^2\right)}{2R_{LIN}}}\left(0.016 + \frac{40}{R_G}\right) + 4. \tag{11.10}$$

If to the above correlation we will insert current value $I_{o,\max} = 20\,\text{mA}$ and relation (11.8), which after transformation gives

$$1 - \frac{R_o\left(At_g + Bt_g^2\right)}{2R_{LIN}} = 1 + \frac{B}{A}t_g, \tag{11.11}$$

then we get relation describes instrumentation amplifier R_G resistor

$$R_G = \frac{40}{\frac{20}{R_o A t_g} - 0.016}. \tag{11.12}$$

In the temperature range analysis, where $t_o = 0\,°\text{C}$ and $t_g = 400\,°\text{C}$ resistors R_{LIN} and R_G have values

$$R_{LIN} = -\frac{1}{2} R_o \frac{A}{B}\left(A + Bt_g\right) =$$

$$-\frac{1}{2}100\frac{3.908\cdot 10^{-3}}{\left(-0.5802\cdot 10^{-6}\right)}\left(3.908\cdot 10^{-3} - 0.5802\cdot 10^{-6}\cdot 400\right) = 1238\,\Omega$$

$$R_G = \frac{40}{\frac{20}{R_o A t_g - 0.016}} = \frac{40}{\frac{20}{100\cdot 0.5802\cdot 10^{-6}\cdot 400} - 0.016} = 357\,\Omega.$$

Precision resistors with determined values should be used in transducer and if it is needed the circuit should be calibrated. To calibration procedure can be used Pt100 platinum resistor simulator.

Signal insensitivity on line resistance changing is experimentally taken. Transducer can be supplied by voltage in range from 9 V to 40 V. The highest temperature value is the transducer parameters are less sensitive on transmission line resistance changing.

Where line resistance has 100 Ω and transducer is supplied by ±15 V voltage then the line resistance 50 Ω increase causing an additional error about 0.1 % and this error is fast rising. When the transducer is supplied by 35 V voltage then the line resistance 350 Ω increase causing an additional error about 0.1 %. Analysing transducer making possible sensor characteristic linearization on 0.1 % level, so meet requirements putted in measurement task.

Example 2.

Design a system for measuring stress in the generator shaft localized in the wind farm. As sensors use strain gauges in bridged mode. Bridge output voltage with a maximum turn shaft is 10 mV. The maximum stress in the shaft frequency is 10 Hz. The signal from the measuring system will be processed using the digital measurement system with a nominal input voltage of 1V. The temperature of the shaft and the same strain gauges and the amplifier is changed in the range of 20 °C ± 20 °C. Determine gain of amplifier, select the type of amplifier, design measurement system, estimated processing errors, and propose a procedure to minimize amplifier processing errors (analog measurement circuit.)

Amplifier (transducer) cooperating with strain gauge bridge should have appropriate gain, high input resistance and high CMRR rate. Amplifier gain was determined based on data from the relation

$$A_u = \frac{e_o}{e_T} = \frac{1}{10}\frac{\text{V}}{\text{mV}} = 100\frac{\text{V}}{\text{V}},$$

where: e_o - amplifier output voltage equal to measurement system input voltage,

e_T - strain gauge bridge output voltage.

On the basis of table 11.1, where the instrument al amplifiers parameters was shown, to processing voltages from strain gauges was chosen AD624 amplifier, because:

- contains resistors net, which allow to get the amplification of 1, 100, 200, 500, 1000,
- low power consumption,
- high value of CMRR,
- short time setting the output signal.

The scheme of instrumentation amplifier AD624 is presented in Fig. 11.2.

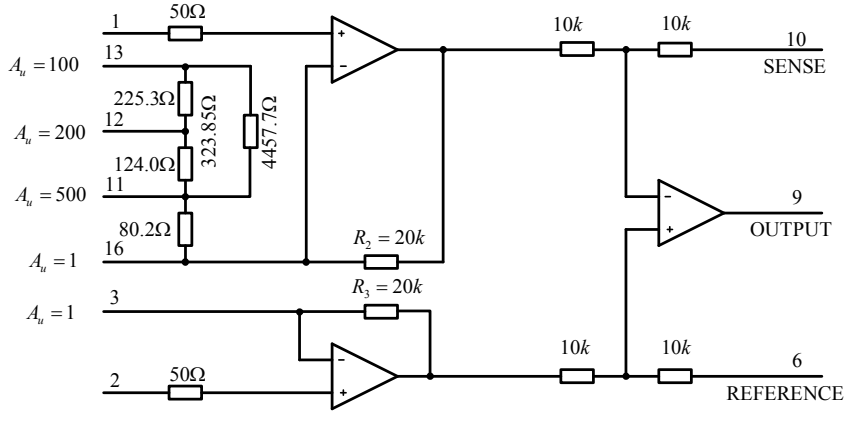


Fig. 11.2. AD 624 instrumentation amplifier scheme

Table 11.1. Chosen parameters of operational amplifiers

Parameter	unit	AMP-01	AMP-05	PGA200	LH0084C
Supplies					
Max.	V	±18	±18	±18	±18
Min.	V	±4.5	±4.5	±10	±8
Supply current (+ve)	mA	4.8	10	10	12
DC offset errors					
Input offset voltage (25°C)	μV	40	500	25	300
Input offset voltage drift	μV/°C	0.3	7	1	10
output offset voltage (25°C)	mV	2	5	0.2	0.6
output offset voltage drift	μV/°C	50	70	10	20
Input bias current (25°C)	nA	2	0.03	10	150
Input offset bias current	nA	0.5	0.01	10	50
Noise					
Input 0.1 to 10Hz (pK pK)	μV	0.12	4	0.8	7
Input density (1kHz)	$nV/\sqrt{H_3}$	5	16	13	-
Input impedance					
Differential	GΩ	1	-	10‖3pF	100
Common mode	GΩ	20	1000‖8pF	10‖3pF	100
Gain					
Range	V/V	0.1-10000	0.1-2000	1-1000	1-100
Accuracy	%	0.5	0.4	0.02	0.03
Drift	ppm/°C	5	8	10	1
Non-linearity	ppm	7	200	120	20
CMRR at dc					
Gain=1	dB	90	80	95	80
Gain=1000	dB	125	100	120	-
Dynamic					
Slew rate	V/μs	4.5 (G=10)	7.5 (G≥10)	0.4	13
3dB bandwidth G=1	kHz	570	3000	500	3250
1% error bandwidth G=1	kHz	-	-	50	300
3dB bandwidth G=1000	kHz	26	120	2.4	-
1% error bandwidth G=1000	kHz	-	-	0.3	-
Settling time 0.1% G=1	μs	12	5	35	2.3
Settling time 0.1% G=1000	μs	50	5	480	-
Comments		Bipolar input. Requires two external gain set resistors	FET input. Requires two gain set resistors. Contains two independent guard drivers	Bipolar input. Digitally controlled, For gains of 1,10 and 100, with three input channels	Bipolar input. Pin strap for gains of 100, 200, 400, 500, 1k, 2k. Contains a single guard driver

Table 11.1 (continued)

INA105	INA101	AD624	AD625	
±18 ±5 1.5	±20 ±5 6.7	±18 ±6 3.5	±18 ±6 3.5	General powered from ±15V supplies.
- - 0.05 5 - -	125 2 0.45 20 15 15	200 2 5 50 50 35	50 1 4 20 30 2	DC offset can usually be terminated to zero with a small pot. Temperature drifts are more difficult do eliminate. Offset and noise can be split into two components one at the input (V_{IO}) and one at the output (V_{OO}) Total input error = V_{IO}= V_{OO}/G.
2.4 60	0.8 13	0.2 4	0.2 4	
50kΩ 50kΩ	10||3pF 10||3pF	1||10pF 1||10pF	1||4pF 1||4pF	FET for high source impedances. Input capacitance dominates about 100Hz.
1 0.005 1 2	1-1000 - - 22	1-1000 0.25(G=100) 25 50	1-10000 0.035 5 100	Many amplifiers require external gain set resistors. Accuracy and drift specifications do not cover this resistors. Generally, non-linearity increases with gain.
90 -	85 105	70 110	75 115	CMRR increases with gain. CMRR is worst at high frequencies.
3 1000 - - - 4 -	0.4 300 20 2.5 0.2 30 350	5 1000 - 25 - 15 75	5 650 - 25 - 15 75	Slew rates and settling time concern large signal changes. Bandwidth figures are for small signals. Generally, larger the gain, the slower the response.
Fixed gain of unity. Standard single op-amp differential circuit.	Bipolar input. Set gain by one extra resistor. Three op amp circuit.	Bipolar input. Contains internal resistors for gains of 1, 100, 200, 500, 1000.	Bipolar input. Gain set by three external resistors. Programmable gain with a differential multiplexer.	

Choice of the AD624 amplifier feedback resistors

Fig. 11.3a shows an AD624 amplifier input circuit, configured for gain $A_u = 100\,\mathrm{V/V}$. Fig. 11.3b presents the resistor net forming the resistor R_1.

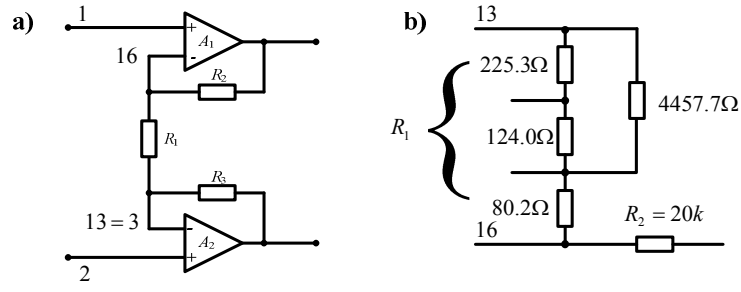


Fig. 11.3. AD624 input circuit
a) the input circuit configuration, b) the resistors net forming the resistor R_1

According to connections shown in Fig. 11.3a the value of the resistor R_1 is

$$R_1 = 80.2 + \frac{(225.3 + 124.0)4445.7}{225.3 + 124.0 + 4445.7} = 404.05\,\Omega .$$

Instrumentation amplifier amplification is

$$A_u = 1 + 2\frac{R_2}{R_1} = 1 + 2\frac{20000}{404.05} = 99.9976\ \mathrm{V/V} .$$

Therefore the amplifier gain is

$$A_u \approx\sim 100\ \mathrm{V/V} .$$

Next, the measurement circuit shown in Fig. 11.4 was accepted, where the tension in the diagonal bridge $e_T = 10\,\mathrm{mV}$ occurs at a maximum torsion of the shaft and the assumption that the resistance strain gauges in the initial state is $R_T = 120\,\Omega$, and the bridge supply voltage is equal to $U_Z = +5.00\ \mathrm{V}$.

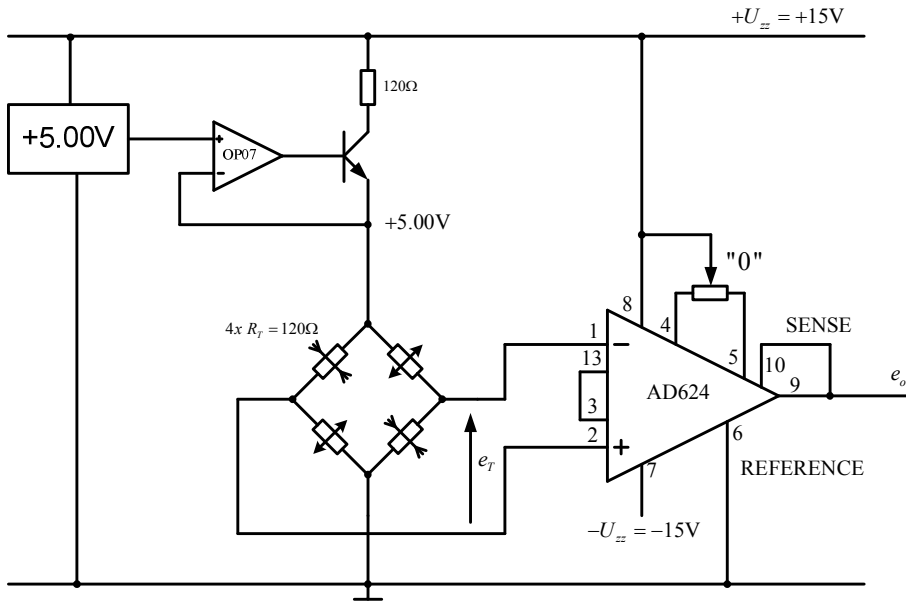


Fig. 11.4. A measurement circuit scheme

Determination of processing errors in the measurement system

1. Gain error

Maximum value of amplifier gain is $\delta A_{\max} = 0.25\,\%$ (Table 11.1), we assume $\delta A_u(R) = 0.1\,\% = 1000$ ppm.

2. Gain drift changes

Catalog data: $\delta A_u(T)/\Delta T = 10\ \text{ppm}/^0\text{C}$, ambient temperature changes by $\Delta t = \pm 20\ ^\circ\text{C}$

$$\delta A_u(T) = \frac{\delta A_u(T)}{\Delta T}\Delta T' = {}^{10\text{ppm}}\!/_{^0\text{C}} \times 20\ ^0\text{C} = 200\text{ppm} \rightarrow 0.02\,\%.$$

3. Gain non-linearity

Catalog data: $\delta A_u(N) = 0.001\,\%$

$$\delta A_u(N) = 0.001\,\% = 10\ \text{ppm}.$$

4. Input resistance influence for processing error

Amplifier input resistance $R_{we} = 10^9\ \Omega$.

Bridge resultant resistance $R_T = 120\,\Omega$

$$\delta R_T = \frac{R_T}{R_{we}} \cdot 100 = \frac{120}{10^9} \cdot 100 \approx 1 \cdot 10^{-5}\ \% = 0.1\ \text{ppm}.$$

5. Input offset voltage

Catalog data: $V_{os} = \pm 25\ \mu\text{V}$.

This voltage is related to a processing signal $e_T = 10\ \text{mV}$

$$\delta A\left(V_{os}\right) = \frac{V_{os}}{e_T} \cdot 100 = \frac{25 \cdot 10^{-6}}{10 \cdot 10^{-3}} \cdot 100 = 0{,}25\% = 2500\ \text{ppm}$$

6. Input offset voltage drift

Catalog data: $\Delta V_{os} / \Delta T = \pm 0.25\ \mu\text{V} / {}^0\text{C}$

This changes with temperature changes by $\Delta T' = 20\,^\circ\text{C}$ related to e_T signal are

$$\delta A\left(\Delta V_{os} / \Delta T\right) = \frac{\Delta V_{os}}{\Delta T} \cdot \frac{\Delta T'}{e_T} \cdot 100 = 0.25 \frac{10^{-6}}{1} \cdot \frac{20}{10 \cdot 10^{-3}} = 100 = 0.05\,\% = 500\ \text{ppm}$$

7. Output offset voltage

Catalog data: $V_{oso} = \pm\, 2\ \text{mV}$.

This voltage is related to $e_o = 1\ \text{V}$

$$\delta A_u\left(V_{oso}\right) \frac{V_{oso}}{e_{wy}} \cdot 100 = \frac{2 \cdot 10^{-3}}{1} \cdot 100 = 0.2\,\% = 2000\ \text{ppm}$$

8. Input offset current

Catalog data: $I_{os} = \pm 10\ \text{nA}$

This current flows through the bridge resistors causes a voltage drop, which we refer to the voltage present at the bridge diagonal $e_T = 10\ \text{mV}$

$$\delta A_u\left(I_{os}\right) = \frac{I_{os} \cdot \frac{R_T}{2}}{e_T} \cdot 100 = \frac{10 \cdot 10^{-9} \cdot \frac{120}{2}}{10 \cdot 10^{-3}} \cdot 100 = 0.006\% = 60\ \text{ppm}$$

9. Input offset current drift

Catalog data: $\Delta I_{os} / \Delta T = \pm 100\ \text{pA} / {}^0\text{C}$

We are determining the same way as in point 8, whereas the temperature changes $\Delta T' = 20\,^0\text{C}$

$$\delta A_w\left(\frac{\Delta I_{os}}{\Delta T}\right) = \frac{\Delta I_{os}}{\Delta T} \cdot \frac{\frac{R_T}{2}}{e_T} \cdot \Delta T' = 100 \cdot 10^{-12} \cdot \frac{\frac{120}{2}}{10 \cdot 10^{-3}} \cdot 20 \cdot 100 = 0.0012\% = 12\ \text{ppm}$$

10. Common mode rejection ratio

Catalog data: $CMRR_{dB} = 110\ \text{dB}$

Without the unit CMRR factor

$$CMRR_{dB} = 20 \lg CMRR$$

Hence

$$\lg CMRR = \frac{CMRR_{dB}}{20}, \qquad CMRR = 10^{\frac{CMRR_{dB}}{20}}.$$

Amplifier output voltage taking into account gain lines asymmetry is

$$e_o = A_u e_d \left(1 + \frac{A_{us}}{A_u}\frac{e_s}{e_d}\right) = A_u c_d \left(1 + \frac{1}{CMRR}\frac{e_s}{e_d}\right),$$

where: e_d - differential voltage,

e_s - common mode voltage,

A_u - differential gain,

A_{us} - common mode gain

and $CMRR = \frac{A_u}{A_{us}}$.

Above relation was written as

$$e_o = A_u e_d \left[1 + \delta A\left(CMRR\right)\right],$$

Where, to relation (3.50), $\delta A_u\left(CMRR\right) = \frac{1}{CMRR}\cdot\frac{e_s}{e_d}$.

Common mode voltage

$$e_s \frac{5\text{V}}{2} = 2{,}5\text{ V} = \frac{e_1 + e_2}{2} = \frac{2.5 + 2.5}{2} = 2.5\text{ V}.$$

Differential voltage

$$e_d = e_T = 10\cdot 10^{-3}\text{ V}.$$

After substituting data to relation we get

$$\delta A_u\left(CMRR\right) = \frac{1}{CMRR}\cdot\frac{e_s}{e_d} = 100 = \frac{1}{10^{\frac{CMRR_{dB}}{20}}}\cdot\frac{e_s}{e_d} = \frac{1}{10^{\frac{110}{20}}}\cdot\frac{2.5}{10\cdot 10^{-3}}\cdot 100 = 10^{\frac{CMRR_{dB}}{20}}$$

$$\delta A_u\left(CMRR\right) = \frac{10^{0,5}}{10^6}\cdot\frac{2.5}{10\cdot 10^{-3}}\cdot 100 = 0.079\% = 790\text{ ppm}.$$

11. Input voltage noises

Catalog data: $U_{pp} = 0.3\,\mu\text{V}$ in range of $\left(0.1 \div 10\right)\text{Hz}$. In this frequency range are dominating noises, so they are related to e_T voltage.

$$\delta U\left(U_{pp}\right) = \frac{\frac{U_{pp}}{2}}{e_T}\cdot 100 = \frac{\frac{0.3\cdot 10^{-6}}{2}}{10\cdot 10^{-3}}\cdot 100 = 0.0015\% = 15\text{ ppm}.$$

12. Input current noises

Catalog data: $I_{pp} = 60$ pA in range of $(0.1 \div 10)$ Hz . In this frequency range are dominating noises, so they are related to e_T voltage

$$\delta U(I_{pp}) = \frac{\frac{I_{pp}}{2} \cdot \frac{R_T}{2}}{e_T} \cdot 100 = \frac{60 \cdot 10^{-12} \cdot \frac{120}{2}}{\frac{2}{10 \cdot 10^{-3}}} \cdot 100 = 3 \cdot 10^{-60/0} = 0.03 \text{ ppm} .$$

Calculating processing errors

If after circuit mounting and running we will not use any means to reduce processing errors, then the calculating error is

$$\delta A_u = \sqrt{\begin{array}{l} \delta A_u^2(R) + \delta A_u(T)^2 + \delta A_u^2(N) + \delta A_u^2(R_T) + \delta A_u^2(V_{os}) + \\ + \delta A_u^2\left(\Delta V_{os}/\Delta T\right) + \delta A_u^2(V_{oso}) + \delta A_u^2(I_{os}) + \delta A_u^2\left(I_{os}/\Delta T\right) + \\ + \delta A_u(CMRR) + + \delta A_u^2(U_{pp}) + \delta A_u^2(I_{pp}) \end{array}}$$

$$\delta A_u = \sqrt{\begin{array}{l} 0.1^2 + 0.02^2\% = 0.001^2\% + \left(1 \cdot 10^{-5}\right)^2\% + 0.25^2\% + 0.05^2 + 0.2^2 + \\ + 0.006^2\% + 0.0012^2\% + 0.079^2 + 0.0015^2\% + 0.000003^2\% \end{array}}$$

$$\delta A_u = \sqrt{0.121} = 0.35\,\%$$

If we will do:

- amplifier gain calibrating ($\delta A_u(R) \to 0$),
- null amplifier ($\delta A_u(V_{os}) \to 0$, $\delta A_u(V_{oso}) \to 0$, $\delta A_u(I_{os}) \to 0$),
- CMRR factor maximizing ($\delta A_u(CMRR) \to 0$),

and pass over the secondary values components, then the processing error is described by

$$\delta A_u \approx \sqrt{\delta A_u^2(t) + \delta A_u^2(\Delta V_{os}/\Delta t)} = \sqrt{0.02^2 + 0.05^2} = \sqrt{0.0029} = 0.0545\,\%$$

The processing error is reduced by one order.

If to amplifier errors correction, caused by temperature changes and amplifier non-linearity, will be used digital measurement system, then a processing error will be depends from amplifier noises.

$$\delta A_u \approx \sqrt{\delta A_u^2(U_{pp}) + \delta A_u^2(I_{pp})} = \sqrt{\left(1.5 \cdot 10^{-3}\right)^2 + \left(3 \cdot 10^{-6}\right)^2} = 0.0015\,\%$$

Amplifier errors correction in analog and digital system part reduced processing error by two orders.

REFERENCES

[1] Clayton G., Winder S.: *Operational amplifiers*, Newnes, Oxford, 2003.
[2] Eimbinder J., *Designing with linear integrated circuits*, John Wiley, New York, 1969r.
[3] Graeme J.G., Toby G.E., Huelsman L.P.: *Operational amplifiers, design and application*, McGraw-Hill, New York, 1971.
[4] Karki J., *Understanding operational amplifier specifications*, SLOA011, Texas Instruments, Dallas, 1998.
[5] Kester W., Jung W., *Op AMP structures, Op AMP applications*, Analog Devices, Norwood, 2002.
[6] Kester W., Jung W., *Precision Op AMP, Op AMP applications*, Analog Devices, Norwood, 2002.
[7] Kester W., *Analog to Digital Conversion*, Analog Devices, 2004.
[8] Kitchin Ch., Counts L.: *RMS to DC conversion application guide, Analog Devices*, Norwood, 1986.
[9] Mc Ghee J., Henderson I.A., Kulesza W., Korczynski M.J., *Measurement Data Handling*, Technical University of Lodz, Lodz, 2001.
[10] Lyons R.G., *Understanding Digital Signal Processing*, Pearson Education; 1996.
[11] Morris A.S., *Measurement and Instrumentation Principles*, Butterworth-Heinemann, 2001.
[12] Nawrocki Z., Dusza D., Kosobudzki G, *Metrological analysis of integrated analog RMS converters described by explicit and implicit functions*, Measurement (London). 2009, vol. 42, nr 2, s. 308-313
[13] Sheingold D.H., *Nonlinear circuits handbook*, Analog Devices, Massachusetts, 1976.
[14] Sidor T., *Electrical and Electronic Measurements and Instrumentation*, Pub. AGH, Krakow, 2006.
[15] Tomota M., Sugiyama T., Ymaguchi K.: *An electronic multiplier for accurate power measurements*, IEEE Trans. Instr. and Measurement, vol. IM-17, 1968, No. 4.
[16] Van de Plassche R., *CMOS integrated analog to digital and digital to analog converters*, Kluwer Academic Publishers, 2003.
[17] Wong Y.J., Ott W.E., *Function circuits*, Mc Graw-Hill, New York, 1976.

Books wrote in Polish
[18] Garret P., *Układy analogowe w systemach cyfrowych*, WNT, Warszawa, 1981.
[19] Golde W., Śliwa L., *Wzmacniacze operacyjne i ich zastosowania*, WNT, Warszawa 1982.
[20] Guziński A., *Liniowe elektroniczne układy analogowe*, WNT, Warszawa, 1993.
[21] Jakubiec J., Roj J., *Pomiarowe przetwarzanie próbkujące*, Wyd. Pol. Śląskiej, Gliwice, 2000.
[22] Miłek M., Metrologia Elektryczna wielkości nieelektrycznych, Of. Wyd. Uniw. Zielonogórskiego, Zielona Góra, 2006
[23] Nadachowski M., Kulka Z., *Analogowe układy scalone*, WKiŁ, Warszawa, 1983.
[24] Nawrocki W., *Komputerowe Systemy Pomiarowe* (Computer Measurement Systems), WKiŁ, Warszawa, 2006.
[25] Nawrocki Z., *Analiza metrologiczna układów logarytmujących i wykładniczych*, Prace Naukowe Inst. Maszyn, Napędów i Pomiarów Elektrycznych Pol. Wrocławskiej Nr 59, Wrocław, 2006.

[26] Nawrocki Z., Wzmacniacze operacyjne i przetworniki pomiarowe, Of. Wyd. Pol. Wrocławskiej, Wrocław, 2008.
[27] Niedźwiecki M., Rasiukiewicz M.: *Nieliniowe elektroniczne układy analogowe*, WNT, Warszawa, 1994.
[28] Rak R.J., *Wirtualny Przyrząd Pomiarowy* (Virtual Measurement Instrument), Of. Wyd. Pol. Warszawskiej, Warszawa, 2003.
[29] Świsulski D., *Komputerowa Technika Pomiarowa* (Computer Measurement Technique), PAK, Warszawa, 2005.
[30] Tietze U., Schenk Ch.: *Układy półprzewodnikowe*, WNT, Warszawa, 2005.
[31] Tumański S., *Technika pomiarowa,* WNT,Warszawa, 2007.
[32] Winiecki W., *Organizacja Komputerowych Systemów Pomiarowych*, Of. Wyd. Pol. Warszawskiej, Warszawa, 1997.

Web pages
[33] www.ni.com – National Instruments.
[34] www.analog.com – Analog Devices.
[35] www.ti.com – Texas Instruments.
[36] www.national.com – National Semiconductors.
[37] www.zigbee.org – Zig Bee Alliance.